TB-A7-200T-IMG
Hardware User Manual

Rev. 2.04

Revision History

Version	Date	Description	Publisher
1.00	2015/05/08	Initial Release	RH
1.99	2015/08/31	Updated. Released.	ST
2.00	2015/09/17	Updated following review.	ST
2.01	2015/09/30	Updated following review.	Morita Odajima
2.02	2015/09/30	Updated with additional dimensions on top dimension drawing	ST
2.03	2015/10/1	Updated with additional dimensions on bottom dimension drawing	ST
2.04	2015/10/9	Updated with additional dimensions on bottom dimension drawing	Morita Odajima

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Introduction and Product Safety

Thank you for purchasing the **TB-A7-200T-IMG** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and always keep it handy.

SAFETY PRECAUTIONS

Be sure to follow these precautions

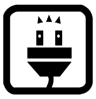
Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to ensure proper use.**
- **These precautions contain serious safety instructions that must be followed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

⚠ **Danger**	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
⚠ **Warning**	Indicates the possibility of serious injury or death if the product is handled incorrectly.
⚠ **Caution**	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

	Warning
	In the event of a failure, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	If an unpleasant smell or smoking occurs, disconnect the power supply. If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.
	Do not disassemble, repair or modify the product. Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	Do not touch a cooling fan. As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	Do not place the product on unstable locations. Otherwise, it may drop or fall, resulting in injury to persons or failure.
	If the product is dropped or damaged, do not use it as is. Otherwise, a fire or electric shock may occur.
	Do not touch the product with a metallic object. Otherwise, a fire or electric shock may occur.
	Do not place the product in dusty or humid locations or where water may splash. Otherwise, a fire or electric shock may occur.
	Do not get the product wet or touch it with a wet hand. Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	Do not touch a connector on the product (gold-plated portion). Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
⃠	**Do not use or place the product in the following locations.** • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
⃠	**Do not place heavy things on the product.** Otherwise, the product may be damaged.

■ Disclaimer

This product is an evaluation board intended for development of video data with Xilinx® Artix® FPGA. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.
The specification of this product is subject to change without prior notice.
The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

Related documents:

All inrevium documents relating to this board can be downloaded from our website. Please see attached paper on the products.

Xilinx FPGA support documents (may require Xilinx User registration to download):
http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/artix-7.html
DS180: 7 Series FPGAs Overview
DS181: Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics
DS874: ChipScope Integrated Bit Error Ratio Test (IBERT) for 7 Series GTP
UG470: 7 Series FPGAs Configuration User Guide
UG471: 7 Series FPGAs SelectIO Resources User Guide
UG472: 7 Series FPGAs Clocking Resources User Guide
UG473: 7 Series FPGAs Memory Resources User Guide
UG474: 7 Series FPGAs Configurable Logic Block User Guide
UG475: 7 Series FPGAs Packaging and Pinouts Product Specifications User Guide
UG479: 7 Series FPGAs DSP48E1 Slice User Guide
UG480: 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-bit 1MSPS Analog-to-Digital Converter User Guide
UG482: 7 Series FPGAs GTP Transceivers User Guide
UG483: 7 Series FPGAs PCB Design Guide
UG586: Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions v2.3 User Guide
UG769: LogiCORE IP 7 Series FPGAs Transceivers Wizard v2.6 User Guide

In addition to the ACDC A7 Carrier card, the following table outlines the included accessories.

Table 1-1 Accessories

Description	Manufacturer	Quantity
Desktop power adapter (40W, 12V, PN: GST40A12-P1J) or equivalent	Mean Well	1
Cable, 0.91m, 18AWG, NEMA 5-15P to IEC320-C13 or equivalent	Tripp Lite	1
Cables, 1.83m, USB A male-MicroB Male	Tripp Lite	2
Standoffs, 35mm, M2.6	Hirosugi	6
Spacer w/ Brass Screw, 35mm, M2.6	Hirosugi	6

2. Overview

The TB-A7-200T-IMG development board for the Xilinx Artix-7 FPGA is a reduced cost platform for evaluating and developing designs targeting Artix-7 FPGAs. Revision 2.0 of this board provides a fansink cooled FFG1156-package -2 speed-grade device.

The base platform common feature set includes:

- Xilinx® Artix®-7 FPGA device:
- Two VITA-57.1 high-pin count FPGA mezzanine cards (FMC) connectors with many I/O and 8 multi-gigabit transceivers (MGT's) available on each
- 2GB DDR3 SO-DIMM module
- 100/1000MBaseT Ethernet RJ45-style port
- Digital Audio S/PDIF coaxial TX and RX jacks
- Micro-USB port for FPGA configuration
- Micro-USB UART port
- 4 general purpose pushbuttons and LEDs, 8-positions general purpose DIP switches
- On-board programmable clock generator
- User clock input MMCX jacks
- 256Mb QSPI Flash for configuration and user data
- Two Digilent Pmod™[1] 12-pin peripheral sockets

[1] *'Pmod' is a trademark of Digilent Inc. The Pmod Interface Specification is the property of Digilent Inc.*

3. Features

FPGA	**Xilinx** Artix-7 XC7A200T -2 speed grade in FFG1156 package, fansink cooling
Memory	**Single** 204-pin 64-bit DDR3 SODIMM slot **256Mbit** Quad SPI Flash **EEPROM** 2K-bit manufacturing information
Clocks	**On-board:** Silicon Labs Si5338B 4-channel clock generator with 25.0000MHz crystal reference
Interfaces	**FMC** VITA-57.1 Connectors:2 x Samtec ASP-134486-01 400-pos HPC socket [2]. Featuring four VADJ voltage settings--1.5/1.8/2.5/3.3V for each FMC. Setting via headers/jumpers. **RJ45** jack for Marvell 88E1116R Gigabit-Ethernet Transceiver, RGMII interface, three status LEDs on PCB **S/PDIF** Digital Audio coaxial jacks, RCA 75-ohms, separate TX and RX via 20Mbps line driver and receiver **MMCX** receptacle pair for external differential clock **XADC** 6-pin header, two channel **Micro-USB** user UART interface via Silicon Labs CP2103-GM **Micro-USB** to JTAG configuration link via Digilent 410-308-P **DC** Barrel jack 2.0/5.5mm for 12VDC, filtered and fuse protected **Power** switch, 2-pos. slide switch, optional header for remote switch (in parallel) **Fan** header 3-pin ATX-pinout 12V, Tach connection **User** push switches, four on each PCB side, parallel wired **User** LEDs, Green, four on each PCB side, parallel wired **DIP** switches, two 4 pos., actuating 8 GPIOs **Pmod** compatible 2x12 PCB edge sockets, 2 sets **JTAG** header Xilinx standard 14-pin 2mm with keyed shroud
Optional	**Power** ON-OFF remote switch header, 2-pin

[2] Refer to VITA 57.1 FMC Standard http://www.samtec.com/standards/vita.aspx

4. Block Diagram

The following figure shows the block diagram of TB-A7-200T-IMG:

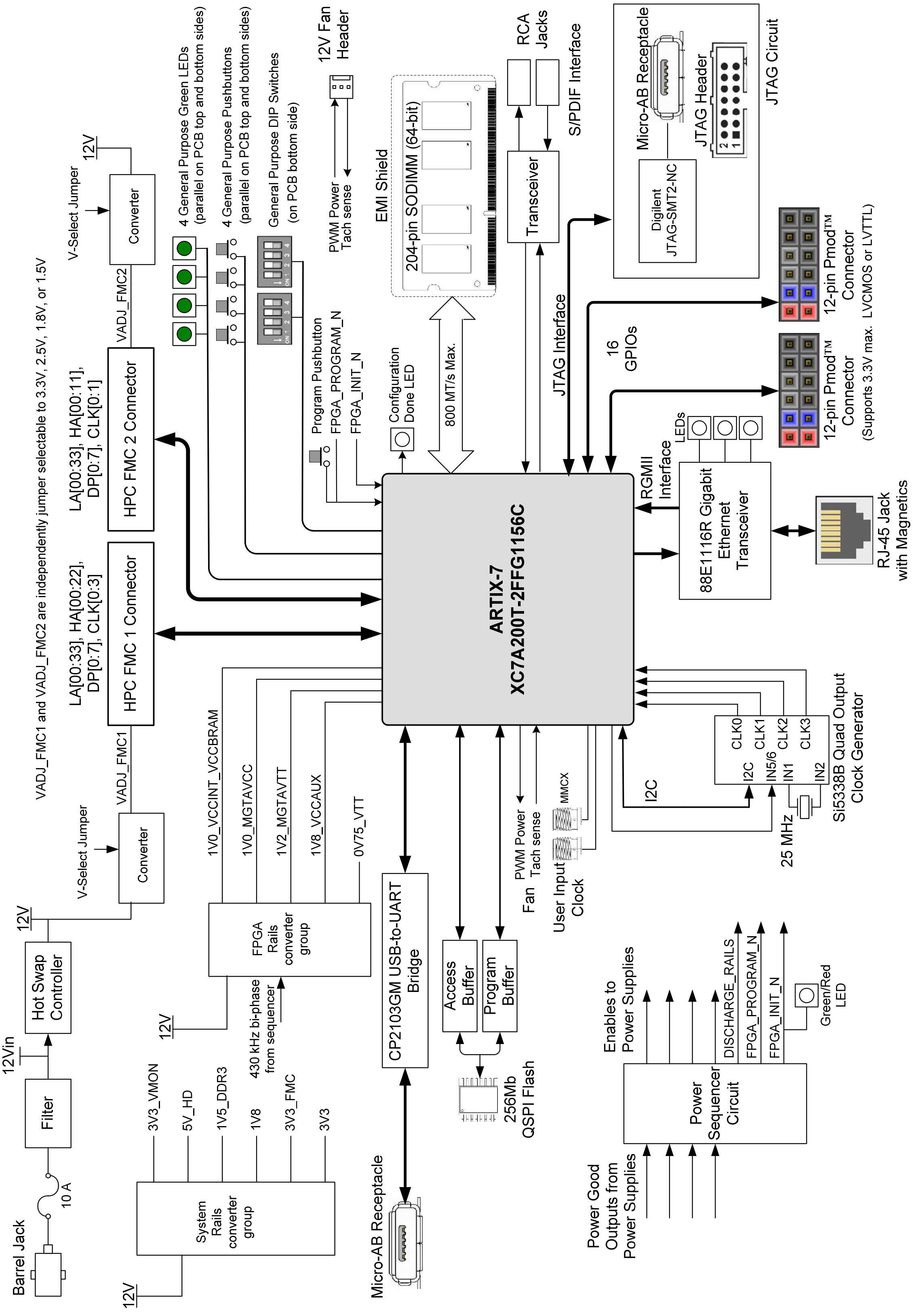


Figure 4-1 Block Diagram

5. External View of the Board

The TB-A7-200T-IMG board's top side components are shown in Figure 5-1.

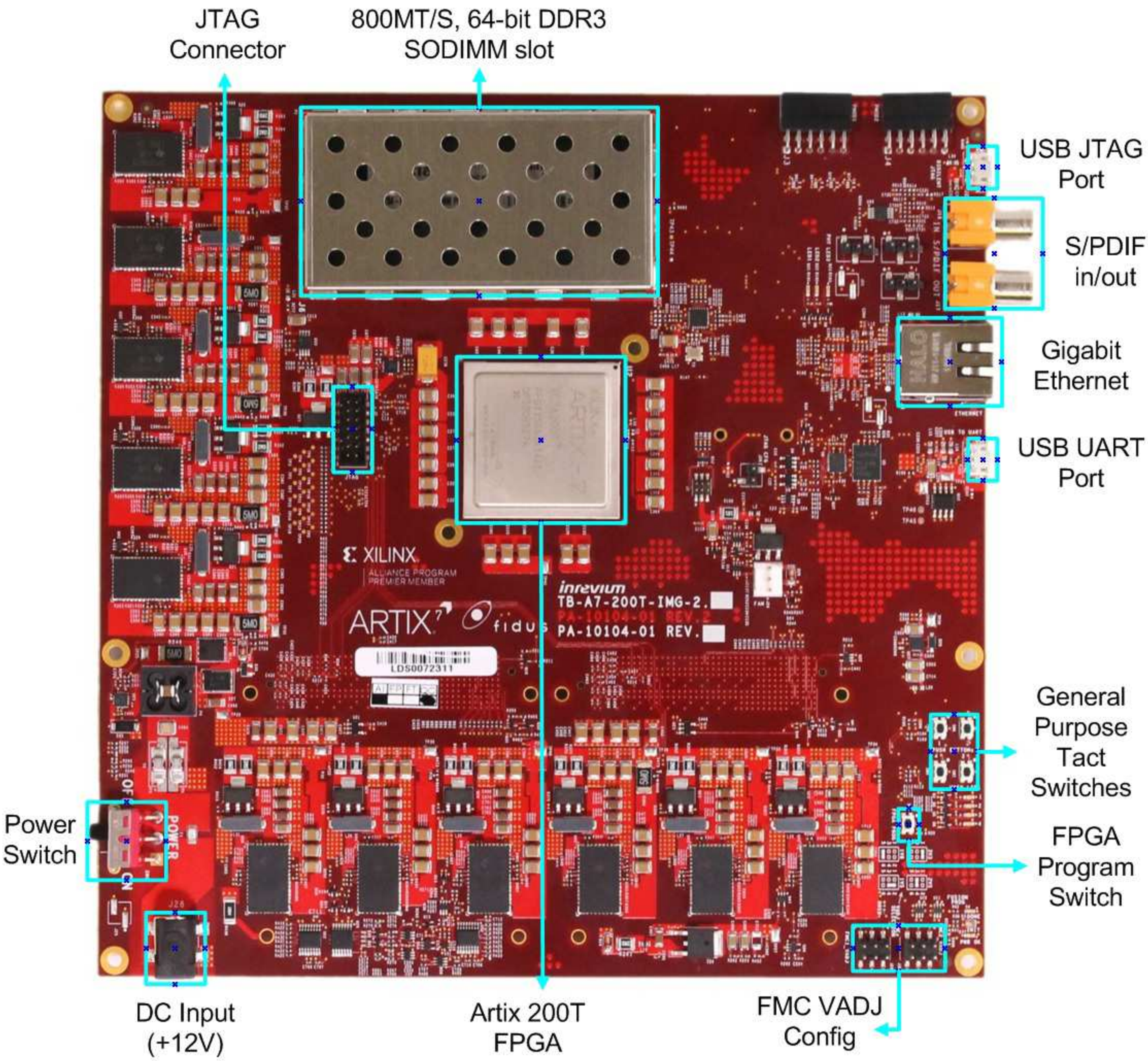


Figure 5-1 TB-A7-200T-IMG Board Top View

The TB-A7-200T-IMG board's bottom side components are shown in Figure 5-2.

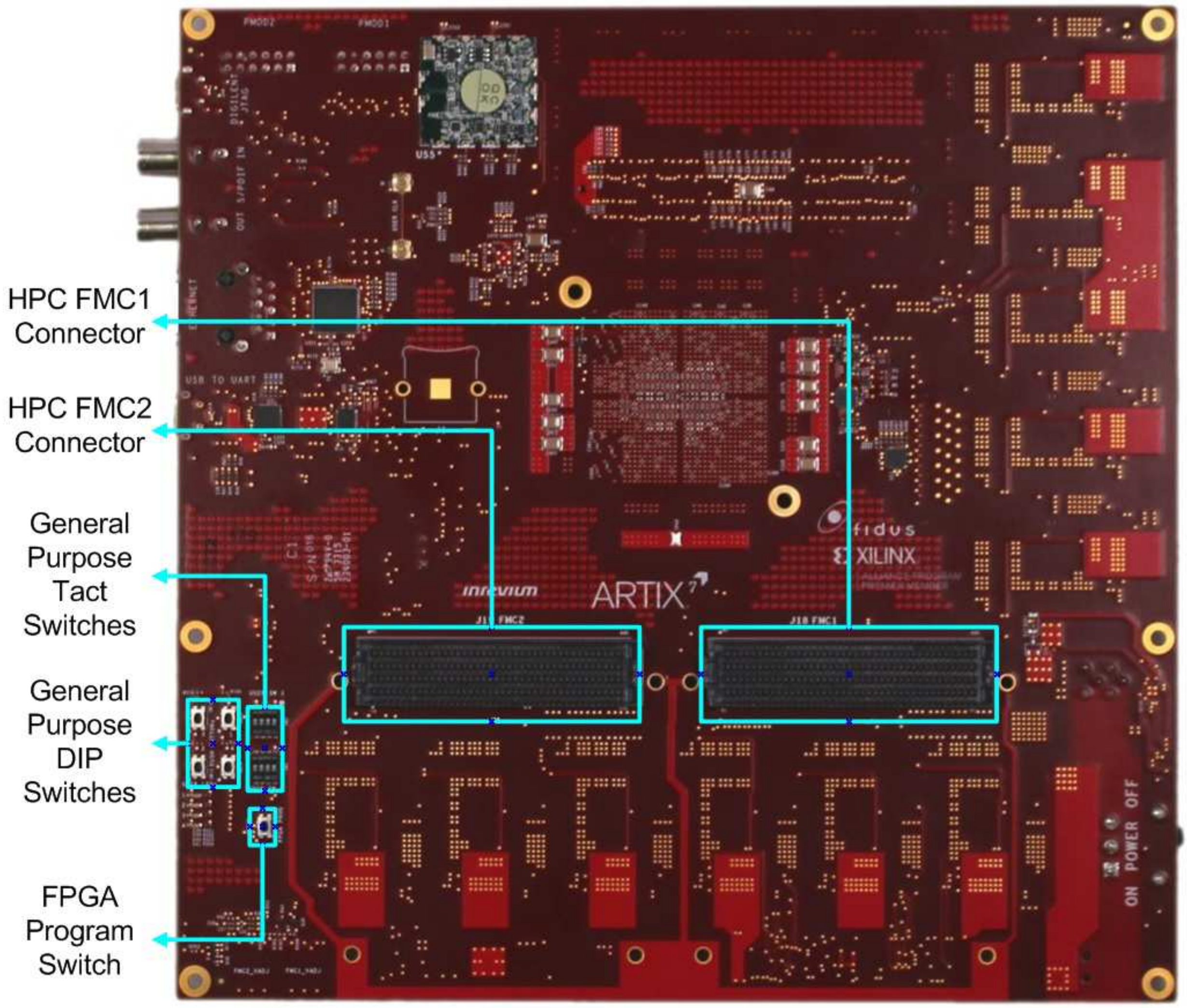


Figure 5-2 TB-A7-200T-IMG Board Bottom View

6. Board Specifications

External Dimensions:	200 mm (W) x 200 mm (H)
Number of Layers:	16 layers
Board Thickness:	2.964 mm +/- 10%
Material:	FR-4
FPGA:	Xilinx Artix-7 XC7A200T-2FFG1156C (35mmx35mm BGA package)
Included Connectors:	
FMC HPC CC Connector:	Samtec ASP-134486-01 10x40-pos. 10mm stacking height
SODIMM Connector:	TE Connectivity 2-2013289-1
Ethernet Connector:	HALO HFJ11-1G01ERL GigE integrated magnetics RJ45 8P8C, no LEDs
Micro-USB Connector:	Hirose Electric ZX62D-AB-5P8
S/PDIF Connector:	KYCON KLPX-0848A-2-O Orange color RCA jack
MMCX Connector:	Molex 73415-2063
XADC Connector:	Harwin M20-8760342 2x3-pos. 2.54mm pitch Header
Fansink Connector:	Molex 22-11-2032 3-pos. 2.54mm pitch, latching Header
Power Input Connector:	CUI PJ-002AH-SMT-TR 2.0mm pin, 5.5mm OD
Pmod™ Connectors:	Sullins PPTC062LJBN-RC 2x6-pos. 2.54mm pitch right-angle socket
VADJ select header:	Harwin M20-8760342 2x3-pos. 2.54mm pitch Header
Xilinx JTAG Connector:	Molex 87832-1420 2x7-pos. 2mm pitch shrouded Header

Optional connectors:

Power remote Connector:	Samtec TSM-102-01-T-SV 2-pos. 2.54mm pitch Header

Note: all Header type connectors are vertically oriented unless otherwise noted.

Figure 6-1 shows the board assembly top side details and dimensions:

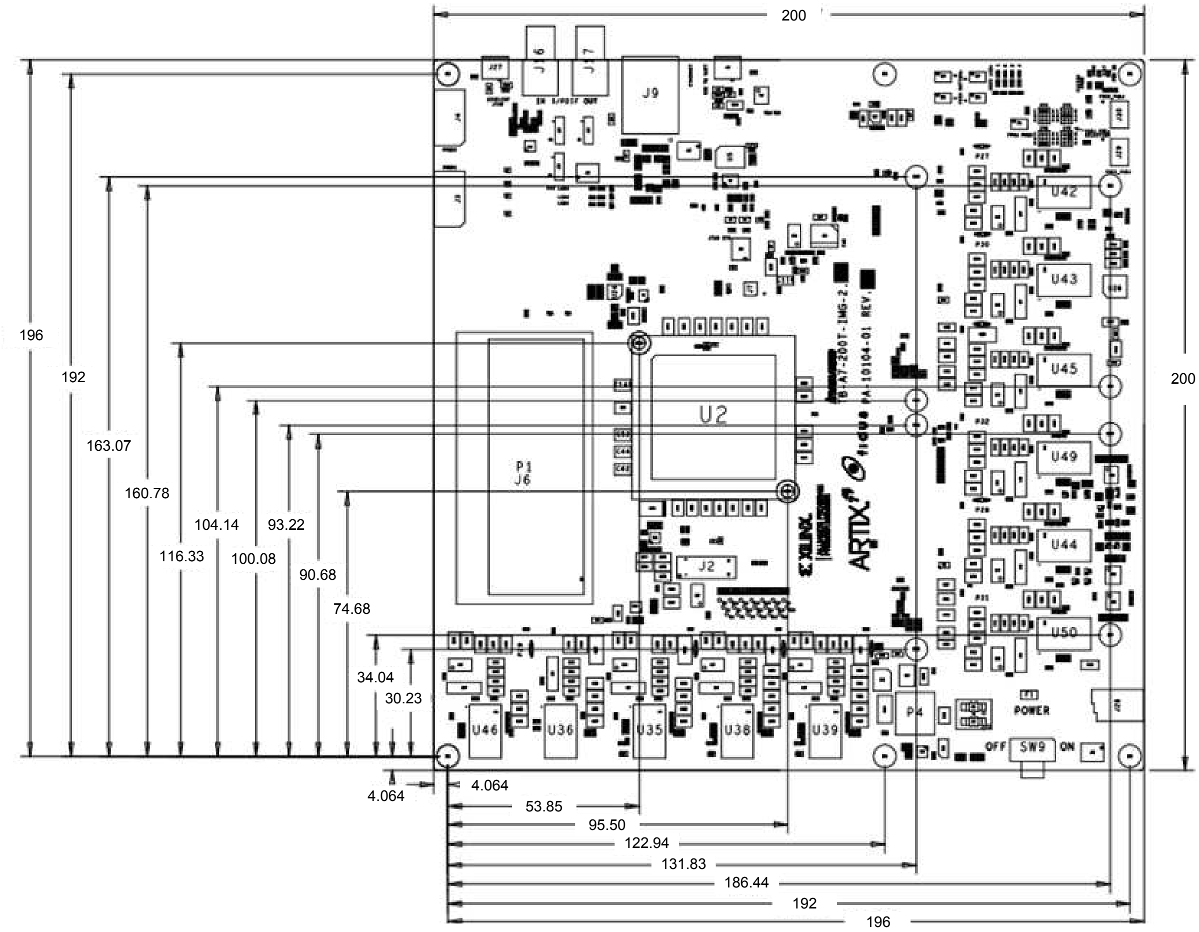


Figure 6-1 Board Dimensions (top view)

Figure 6-2 shows the board assembly bottom side details and dimensions:

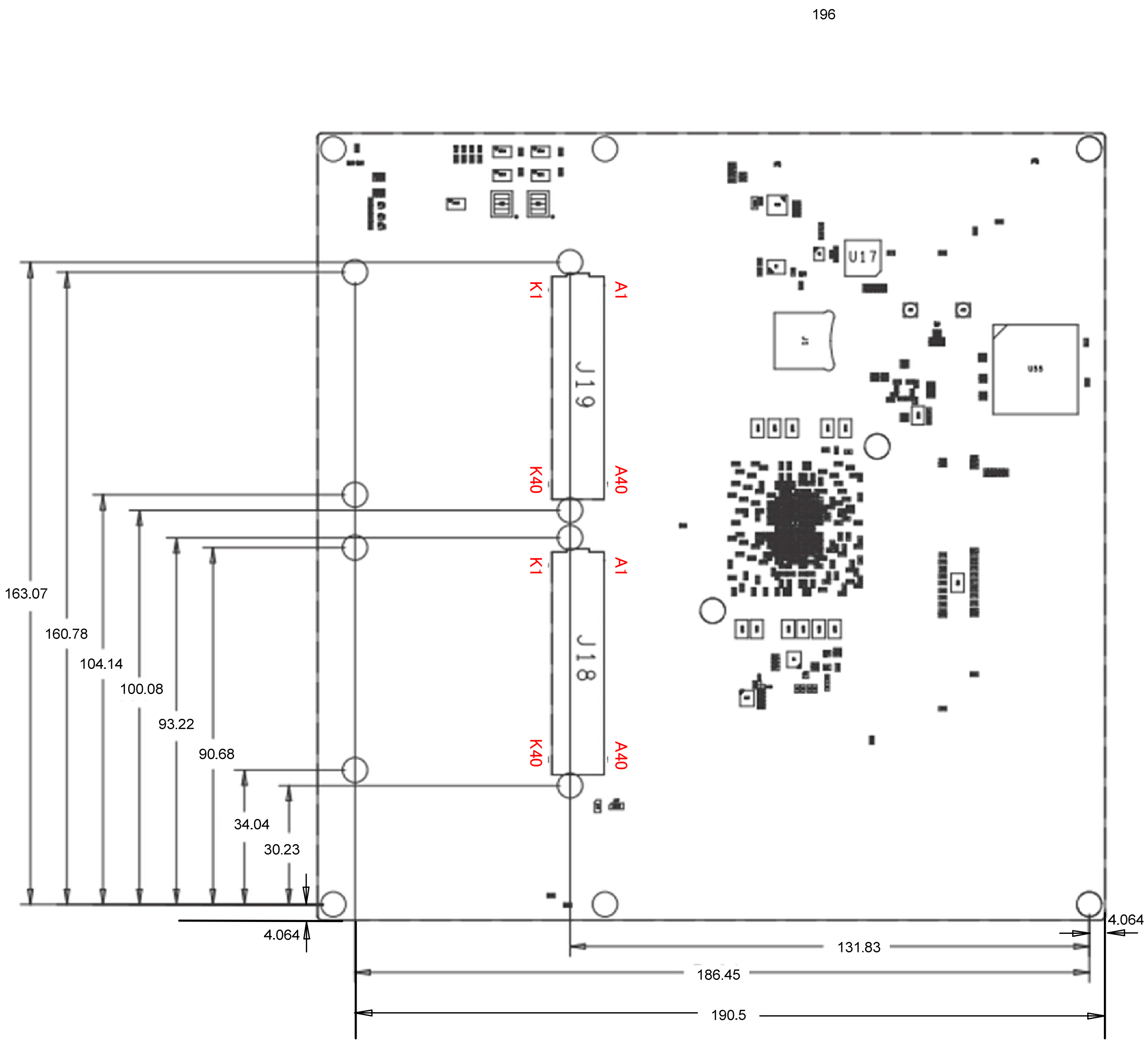


Figure 6-2 Board Dimensions (bottom view)

7. Description of Components

7.1. Power System

The TB-A7-200T-IMG board's power supply structure is shown in the figure below. The major parts of the power supply system are then discussed.

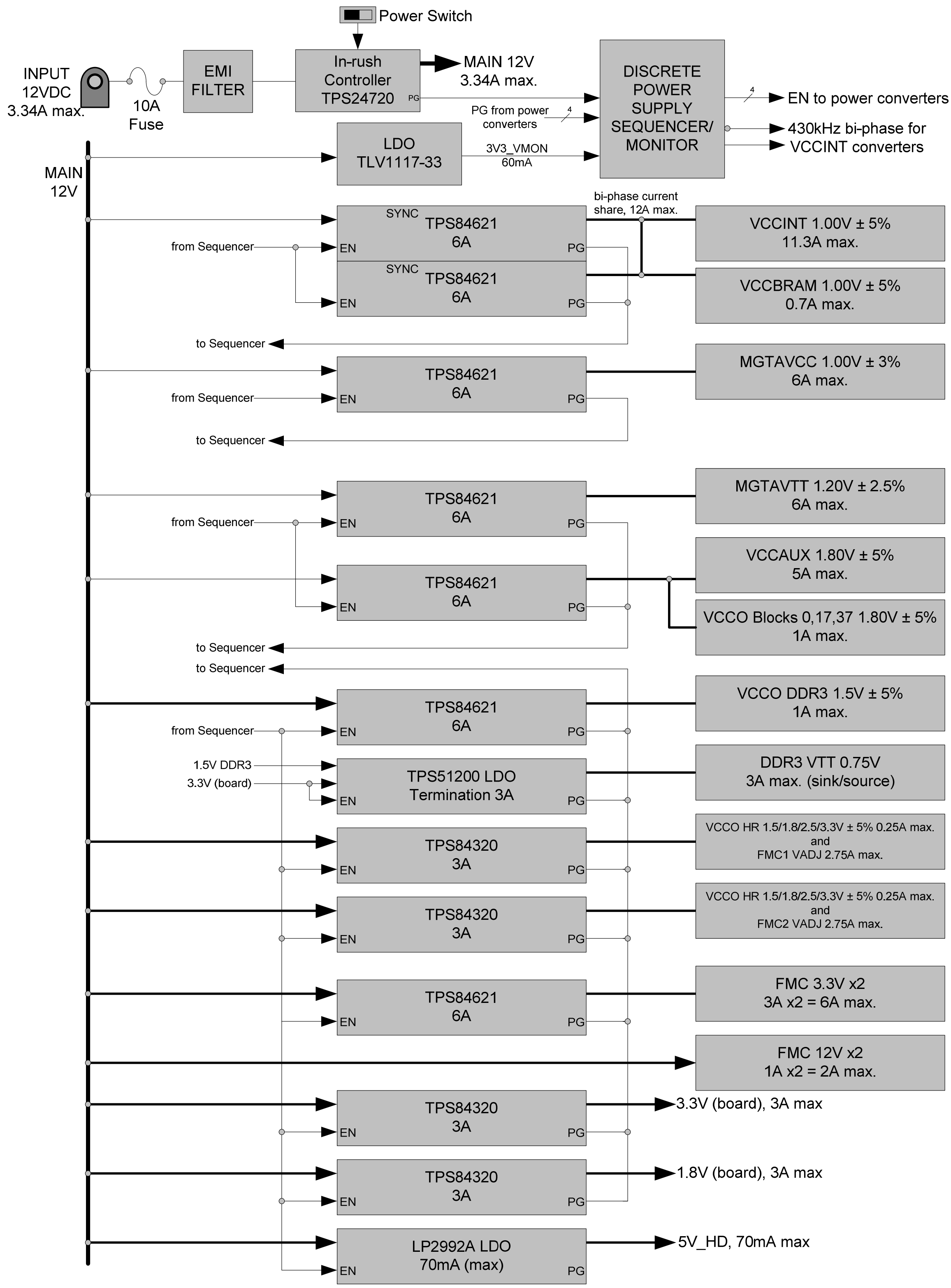


Figure 7-1 Power Supply Structure

7.1.1. Power Input connector

The TB-A7-200T-IMG has a single power input connector on the board, a standard DC power jack with 2.0mm pin and 5.5mm barrel dimensions. Use only the power supply brick specified by inrevium. The center pin is positive and the barrel is negative; the center pin is fuse protected. Both conductors pass through an optional common-mode filter choke array, as well as an EMI filter block, before being applied to board circuitry.

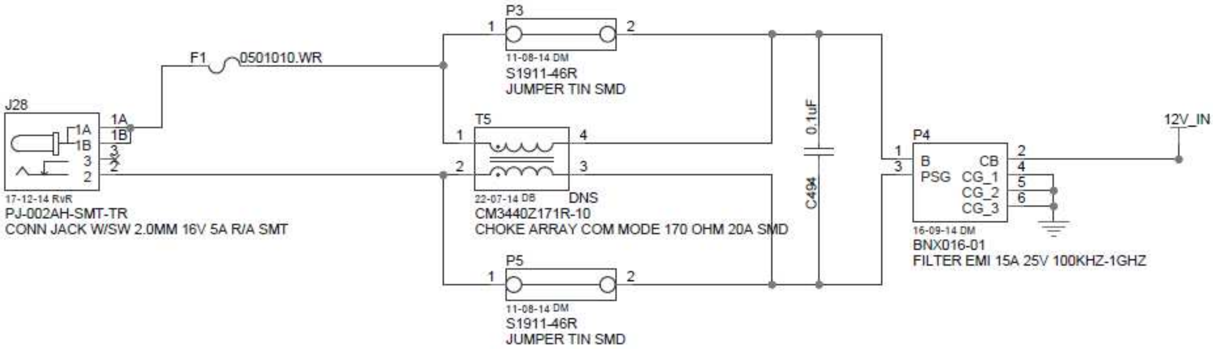


Figure 7-2 Power Input Circuit

7.1.2. Input Power Protection Circuit

The TB-A7-200T-IMG features an input power protection circuit based on the Texas Instruments TPS24720 Hot Swap Controller. This circuit isolates the large distributed capacitance of the board (approx. 2500uF plus as much as 2000uF depending on the two FMC modules), preventing large transient currents from the AC adapter's output capacitors when hot plugged into the board. No more than 100nF of capacitance is directly presented to the adapter output and the in-rush current is ramped up softly, preventing potentially damaging voltage spikes from being produced through the inductance of the DC cord.

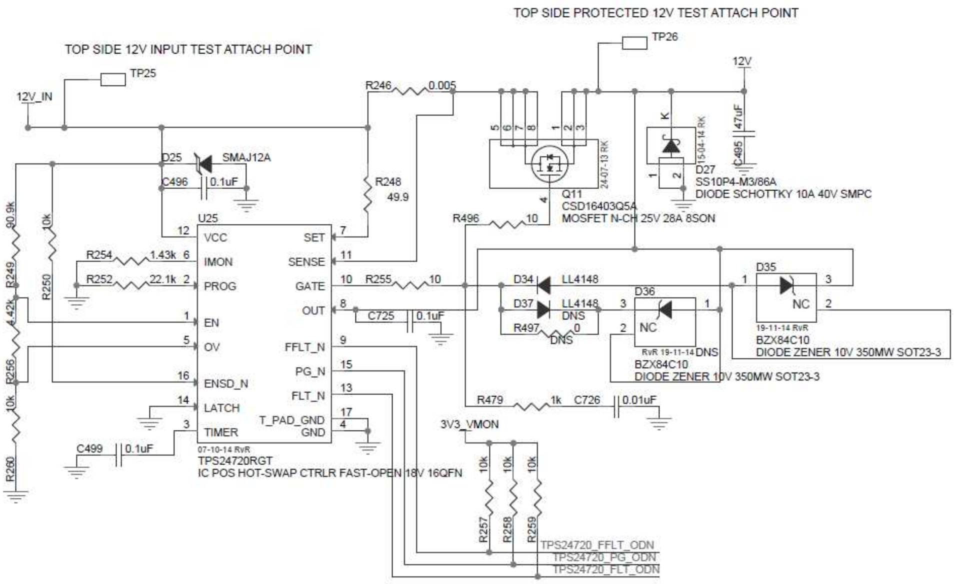


Figure 7-3 Input Power Protection Circuit

The main 12V rail smoothly rises from 0V on either switch-ON or hot plug-in (power switch is the recommended method), requiring approximately 10msec with two maximum capacitance FMC modules installed on the board. The Controller's Under-Voltage detection ensures that the input voltage exceeds 9.8V before enabling, and shuts down on input over-voltages exceeding 14.2V.

7.1.3. Board Power Switch

The TB-A7-200T-IMG also features a system power ON-OFF control that allows the use of a low-current, low voltage SPST switch on the board, or a remote panel or enclosure mounted switch using the optional header (J25 to the right of the switch in the photo below). The slide style switch is shown in the OFF position. The actuator of the switch extends approximately 1.5mm off the edge of the PCB.

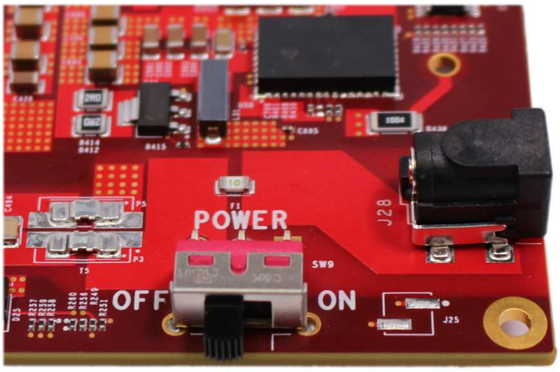


Figure 7-4 Board Power Switch

7.1.4. Power Supply Architecture

The TB-A7-200T-IMG power system consists of eleven high efficiency switching buck regulators and three linear LDO regulators. All regulators except the DDR3 VTT source/sink LDO are powered from the main 12V. The switching regulators can efficiently provide full rated current without additional heat sinking beyond that provided through the PCB coupled cooling.

The switching converters, made by Texas Instruments, are compact integrated modules that contain all but the input and output capacitors. There are only two different TI switching converter types employed on the TB-A7-200T-IMG; the TPS84320 for 3-Amp capacity, and the TPS84621 for 6-Amp capacity. The VCCINT/VCCBRAM converter must supply up to 12Amps to the FPGA core; this supply consists of a pair of 6-Amp TPS84621 converters in a parallel-shared output configuration, using bi-phase synchronization to reduce peak input ripple current. The bi-phase synchronization is achieved through driving the CLK input of each converter with the same frequency at 180-degrees phase shift relative to each other.

Two linear regulators operating from 12V provide 60-80mA of current:

- The 3V3_VMON rail is a system rail generated from the 12V output of the Hot-Swap controller stage (Texas Instruments, TLV1117-33). This rail is primarily used in the power sequence interface logic and must be stable before the power-ON sequence commences Stage 1.
- The 5V_HD regulator also operates from the 12V output of the Hot-Swap controller stage (Texas Instruments, LP2992A). This rail is provided to the XADC header for attached analog signal conditioning circuitry (buffers, filters, differential converter amplifiers, etc.)

A third linear regulator, the Texas Instruments TPS51200, is powered from 1.5V and 3.3V and is used to generate the DDR3 VTT supply. This regulator is specially designed for DDR termination and can both sink and source up to 3-Amps, with its main power path supplied by the output of the 1V5_DDR3 switching regulator.

7.1.5. Power Sequencing

The FPGA requires specific supply rail sequences in order to avoid large transient currents during power-up and power-down. This is achieved using a discrete power sequencing circuit. The circuit accepts “Power Good” indicators from the various DC-DC converters and then sequences the DC-DC converter “Enable” signals appropriately.

7.1.6. Voltage Rails Test Points

The development board features several power rail test points that can be used for debugging or other types of measurements.

Table 7-1 Voltage Rails Test Points

Voltage Rail	Test Point #	Power Supply for
12V_IN	TP25	12V fused and filtered Input Power
12V	TP26	Main Hot-Swap switched 12V rail
3V3_VMON	TP27	Board logic standby rail
3V3_SEQ_CTRL	TP43	Power Sequencer standby rail
1V8	TP33	USB UART, Ethernet PHY 1.8V
1V5_DDR3	TP37	DDR3 and corresponding FPGA Banks
0V75_VTT	TP38	DDR3 SDRAM Termination
1V0_VCCINT_VCCBRAM	TP29	FPGA Core and memory
1V0_MGTAVCC	TP32	FPGA MGTAVCC
1V2_MGTAVTT	TP31	FPGA MGTAVTT
1V8_VCCAUX	TP36	FPGA VCCAUX & VCCAUX_IO
3V3	TP34	Pmod IO, QSPI Flash, Clocks, SPDIF, I2C
5V_HD	TP28	XADC IO accessory rail
3V3_FMC	TP35	FMC1-2 Logic 3.3V rail
5V0_USB_VBUS	TP24	Micro-USB 5V input
5V0_USB_FILT	TP23	Micro-USB filtered 5V
VADJ_FMC1	TP39	FMC1 VADJ rail
VADJ_FMC2	TP40	FMC2 VADJ rail
GND (top)	TP41	Test Ground attach point
GND (bottom)	TP42	Test Ground attach point

7.1.7. Power and Miscellaneous LEDs

Shown below are the different LEDs present on the board which serve as power indication or general purpose programmable LEDs.

Table 7-2 Board LEDs

LED	Color	Used for
D3	Bicolor: Green / Red	FPGA Programming INIT signal Red: Programming in progress Green: Programming complete
D4	Green	FPGA Programming DONE signal
D11 (top), D38 Bottom)	Green	User LED 1
D13 (top), D39 Bottom)	Green	User LED 2
D14 (top), D40 Bottom)	Green	User LED 3
D15 (top), D41 Bottom)	Green	User LED 4
D21	Green	Ethernet LED1 - undefined (default)
D22	Green	Ethernet LED2 - Activity
D23	Green	Ethernet LED3 - Link
D44	Green	All Power Good

7.1.8. FMC VADJ Voltage Selection

The two FMC module positions on the TB-A7-200T-IMG can provide independently selectable VADJ voltage rails to the attached FMC modules. These rails are selected by a pair of 2x3 2.54mm headers that accept a single standard 2-pin shorting shunt on each. The shunts can select one of four voltages which are presented to their respective FMC module receptacles.

The voltages must be determined and shunts installed prior to power-up of the TB-A7-200T-IMG board. Since VADJ1 (FMC position 1) is also used as the power rail for the B0 bank of the FPGA, protective measures are incorporated to ensure the FPGA is not damaged through accidental change or loss of shunts while the board is powered up. The following table outlines the banks powered by each of the two adjustable supplies.

Notes:

1. The VADJ voltages must be set prior to applying power. They must not be changed while the board is powered.
2. The VADJ voltage is determined based on the needs of the FMC module and the respective FPGA bank.

Table 7-3 VADJ connected Banks

VADJ Number	Header	Connected Banks	Voltage
VADJ1	J40	B0, B12, B13 ,B14	1.5/1.8/2.5/3.3V
VADJ2	J41	B15, B16	

The Shunt voltage selection positions for both headers (J40, J41) are shown below:

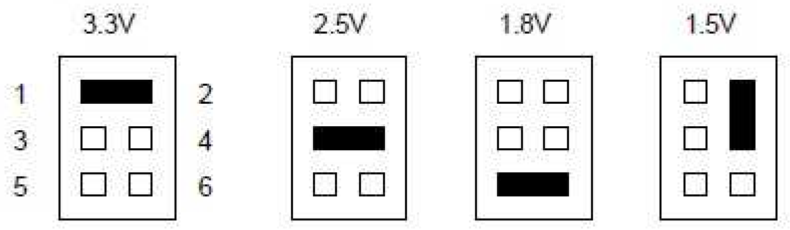


Figure 7-5 VADJ Voltage Selection Header shunt Positions

Note: Only place one shunt (jumper) per header, in a valid, desired configuration above or permanent board damage may occur.

7.2. FPGA Banks Assignments

The TB-A7-200T-IMG supports the Xilinx Artix-7 FPGA in the FFG1156 package. The figures below present the Artix-7 bank structure and user bank function assignments on this board using the XC7A200T:

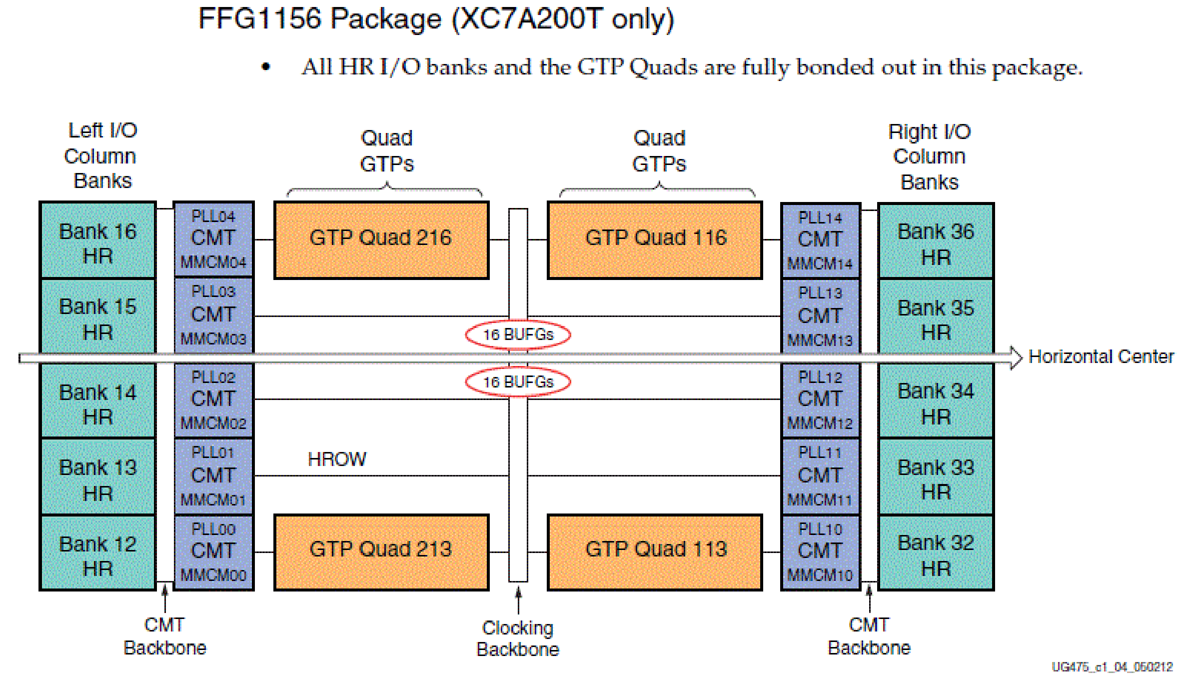


Figure 7-6 XC7A200T-FFG1156 Bank Structure

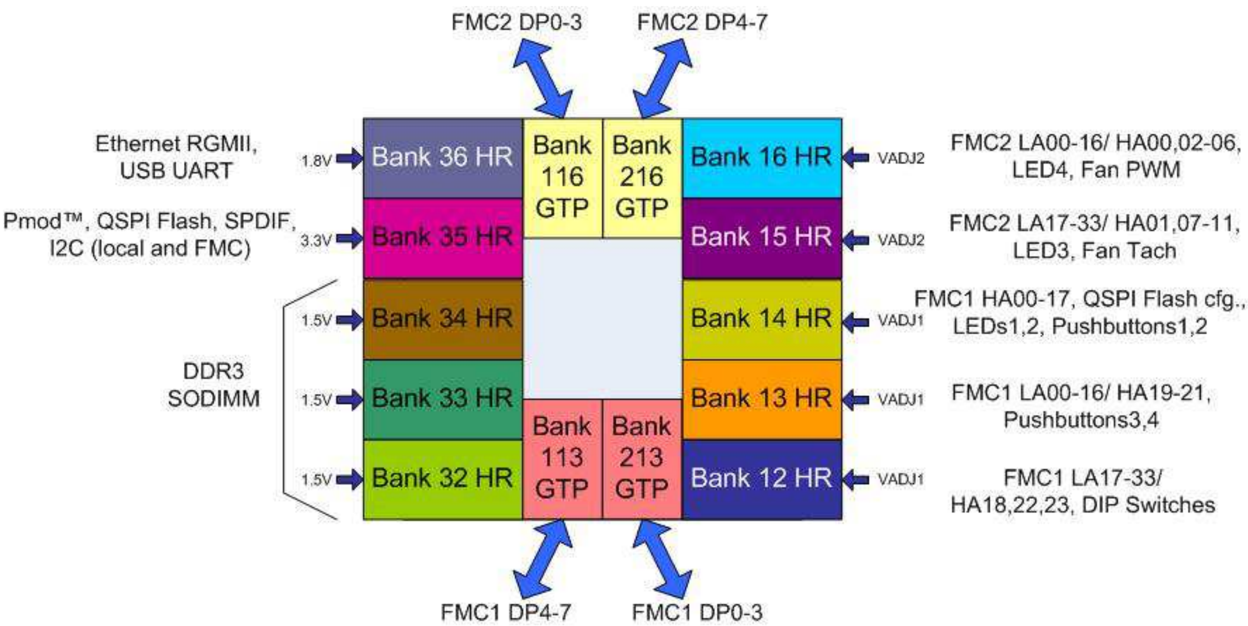


Figure 7-7 TB-A7-200T-IMG User Bank Function Assignments

Notes:

- Bank 0 is the FPGA configuration control bank and is not represented in the User bank function assignment diagram.
- The QSPI Flash connection to Bank 14 is active only during FPGA configuration. User access to the QSPI Flash should be conducted through Bank 35.

7.3. Clock System

7.3.1. Main System Clock generator

The TB-A7-200T-IMG has a single, quad-output programmable clock generator, the Silicon Labs Si5338B, to generate the main board clocks. This device supports an external 25.000MHz crystal as a frequency reference, and can be programmed through an I2C interface to produce a wide range of frequencies independently on the four output channels. Additionally, the type of output driver for each channel can be programmed, and the chip provides independent IO voltage rails for each channel.

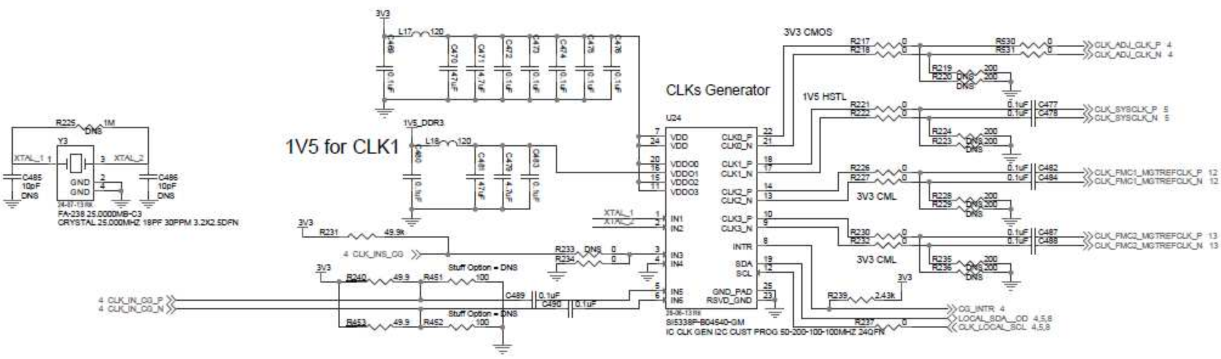


Figure 7-8 Main Clock Generator

An internal one time programmable (OTP) NV memory can be pre-programmed by the chip manufacturer to customer required default frequencies and output types. For this board, the Si5338's OTP NV storage is pre-programmed- the default input source is selected to be the on-chip crystal oscillator and the four outputs are programmed in the following manner:

Table 7-4 Clock Generator Output Details

Output #	Default Frequency	IO Voltage	Output Type	Destination Input
CLK0	50.00MHz	3.3V	LVCMOS	Bank 35 MRCC
CLK1	200.00MHz	1.5V	HSTL	Bank 33 MRCC
CLK2	100.00MHz	3.3V	CML	Bank 213 MGTREFCLK1
CLK3	100.00MHz	3.3V	CML	Bank 116 MGTREFCLK1

Although the device defaults to factory programmed settings, all settings can be modified through the I2C interface. The Si5338B presents a slave address of 0x70h to the local I2C bus hosted from FPGA bank35. Refer to Silicon Labs document Si5338-RM for details on the internal structure and register set.

The user may change any of the clock frequencies to suit application requirements, however, the output types must remain as specified in the preceding table. Note that the FPGA uses its own internal clock for configuration from the SPI Flash and is not dependent upon any of the clocks generated by the Si5338B.

In addition to the crystal oscillator, the Si5338B provides several inputs that can feed the reference or feedback inputs of the first PLL stage phase detector. Inputs 5 and 6, which can operate differentially or single-ended, run from 3.3V FPGA IOs on bank 35. The FPGA IO pair (IO19) can be set for TMDS_33 differential output mode to properly drive the input at up to 350MHz. Alternate termination options in layout can also allow other IO modes. Input 3 is optionally provided as an LVCMOS

single-ended signal from FPGA bank 35, and can serve as an input to the PLL for FPGA based feedback-loop logic.

Notes:

```
# reserved clock (pll.clock_out1)
set_property IOSTANDARD LVCMOS33 [get_ports {clk_adj_clk_p}]
set_property PACKAGE_PIN P5 [get_ports clk_adj_clk_p]

# reference and system clock(pll.clock_out2)
set_property IOSTANDARD DIFF_SSTL15 [get_ports {sysclk_clk_n sysclk_clk_p}]
set_property PACKAGE_PIN AE6 [get_ports sysclk_clk_n]
set_property PACKAGE_PIN AD6 [get_ports sysclk_clk_p]

# Si5338 (pll.clock_in)
set_property IOSTANDARD TMDS_33 [get_ports {clk_out_cg_n clk_out_cg_p}]
set_property PACKAGE_PIN R7 [get_ports clk_out_cg_n]
set_property PACKAGE_PIN R8 [get_ports clk_out_cg_p]
```

7.4. FMC HR IO Clocks

The HR IO clocks are associated with the general logic IOs provided by the FPGA to FMC modules and fall into three categories; module global M2C (Module to Carrier), bank associated CC (bi-directional), and module global BIDIR (bi-directional). BIDIR clocks are available since this board supports HPC type FMC connections. Note that only FMC position 1 supports the BIDIR clocks and they are left unconnected on FMC position 2. Refer to FMC specification ANSI/VITA 57.1 for more details regarding the application of the various clocks.

The HR IO clock signals are all directly DC connected from the FMC clock pins. Users should ensure correct configuration of the clock input type and that terminations are enabled. Users should also be aware that many FPGA HR IO modes are VCCIO (VADJ) dependent, and must insure that the IO standard used can operate at the selected VADJ voltage. Refer to Xilinx document UG471 7-Series SelectIO Resources User Guide for more information.

The HR Ref clock assignments are shown in the following figure:

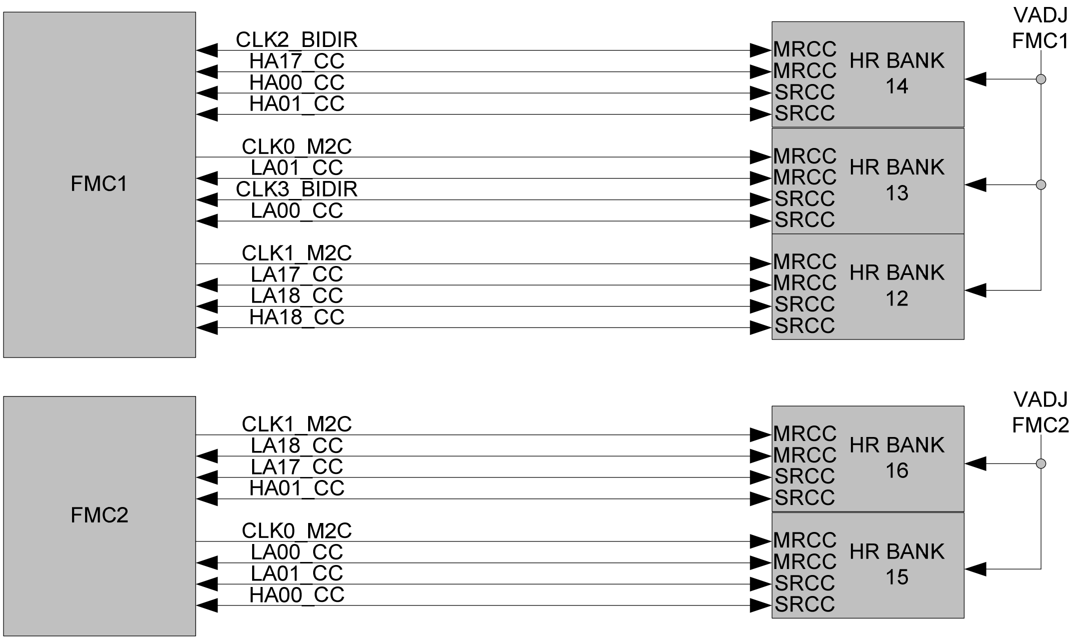


Figure 7-9 FMC HR-IO Clock Assignments

Assignment of FMC global M2C and bank CC clocks to the MRCC and SRCC inputs of their respective banks allows either FMC position to be configured within the FPGA to drive internal multi-regional and global clocking domains. The MRCC inputs in particular can supply direct clocking to multiple regions within the FPGA, and have been assigned with the global M2C clocks from both FMC positions. The bank associated CC clocks of the FMCs supply the more limited SRCC clock inputs that drive the regional logic of the banks assigned to their respective FMC IO groups (LA00-16, LA17-33, HA00-16, HA17-33). Refer to Xilinx document UG472 7-Series FPGAs Clocking Resources User Guide for details on the internal resources and clock distribution capabilities.

7.4.1. FMC GTP Clocks

The GTP clocks are associated with the high-speed differential FPGA serial link blocks, which on the TB-A7-200T-IMG are evenly divided between the two FMC modules (8 per module). All GTP clocks are driven in differential CML mode from the FMC positions as well as the clock generator. The FPGA MGTP ref clock inputs internally provide correct termination of the AC coupled clock signals. The GTP Ref clock assignments are shown in the following figure:

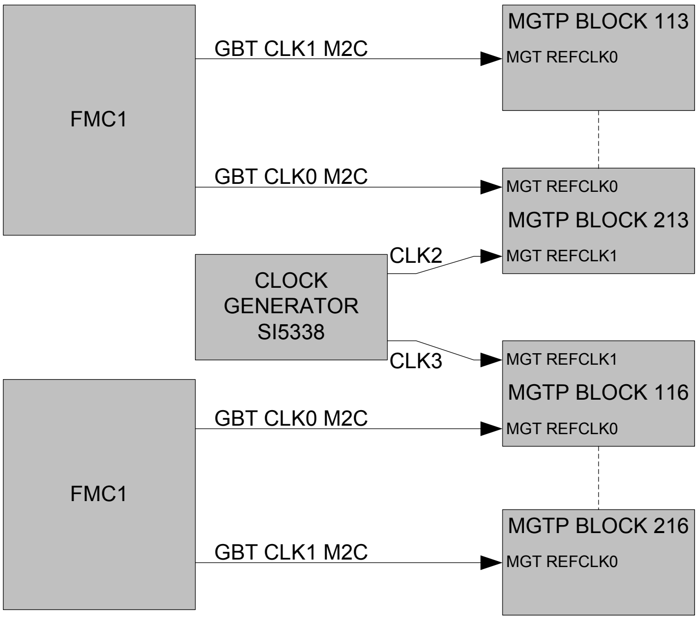


Figure 7-10 GTP Clock Assignments

The Si5338B clock generator shown is the main system clock generator; outputs 2 and 3 are assigned to provide clock reference to the high speed serial links of FMC 1 and FMC 2 respectively, and are programmed to a default frequency of 100MHz. These clocks can be used as a timing reference to the GTP blocks in absence of a ref clock source on the respective FMC module.

7.4.2. User Clocks

Two general purpose user clock sources may drive the FPGA, as depicted below:

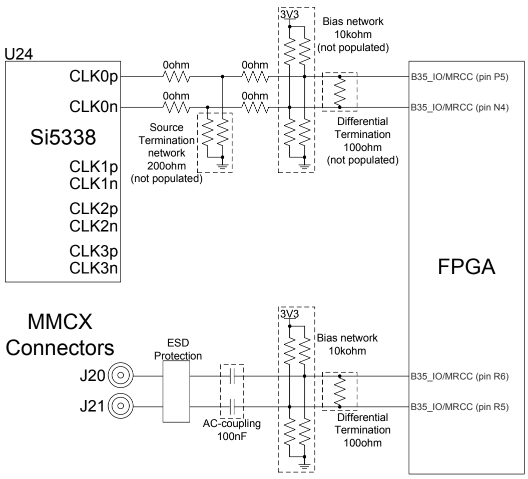


Figure 7-11 User Clocks

1. The CLK0 output of the onboard Si5338 is connected to a global clock input of the FPGA. The default hardware configuration supports a single ended 3V3 CMOS clock.

Note: If required, the user may configure the Si5338 to drive a differential clock input, however, soldering is required. Any soldering voids the warranty.

2. A pair of MMCX receptacles are designed to be driven by an external differential clock source. As per the diagram, the MMCX inputs are provisioned with ESD protection and are AC-coupled. Following the AC-coupling capacitors, the signals are re-biased, and terminated by 100 ohms, as required by the FPGA (due to VCCO=3.3V on that bank).

Note: If required, the user may drive a single ended clock into the MMCX connectors, however, soldering is required. Any soldering voids the warranty.

Note: Prior to driving the MMCX connectors, review Xilinx's guidelines on signal type and maximum amplitude. Incorrect levels, if applied to the MMCX connectors, could permanently damage the FPGA, board, or both.

Note:

```
# connector input clock
set_property IOSTANDARD TMDS_33 [get_ports {user_clk_n user_clk_p}]
set_property PACKAGE_PIN R5 [get_ports user_clk_n]
set_property PACKAGE_PIN R6 [get_ports user_clk_p]
```

7.4.3. DDR3 Clock

Channel 1 of the programmable clock generator drives the MRCC inputs of Bank 33, the middle bank of three assigned to the DDR3 DRAM SODIMM interface. Although the clock can be distributed globally, this clock channel should be reserved exclusively for the DDR3 interface logic and it's frequency determined by the DDR3 operation speed requirements.

7.5. FMC Connector Interface

The TB-A7-200T-IMG board has two high-pin count (HPC) 400 pin FMC connectors (FMC 1 and 2) on board as shown on the block diagram. These FMC connectors follow the VITA 57.1 standard, using Samtec ASP-134486-01 receptacles that accept Samtec ASP-134488-01 (or equivalent) plugs present on FMC modules. The connectors are located beside each other to accept either two single FMC modules or one double width FMC module per VITA 57.1.

Presented below is the ANSI/VITA 57.1 standard pin assignment of high pin count (HPC) FMC connectors.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 7-12 VITA 57.1 FMC HPC/LPC Pinout

Note:

Not all of the IO pins shown in the pinout above are assigned on the TB-A7-200T-IMG FMC connectors. The pin assignment conforms to the VITA 57.1 mandated progression of LAxx population followed by HAxx and HBxx, in increasing numeric order. Please refer to the following FMC connector to FPGA IO pin mapping tables for details on the two FMC FPGA IO assignments of the board.

7.5.1. FMC HPC 1 (J18) IO Allocation

This FMC connects all 34 LAxx differential pairs and all 24 HAxx differential pairs to banks on the FPGA. HBxx ports are not connected. Eight high-speed DP lanes are provisioned with GTP pairs (TX and RX) and both GBT Clocks are received.

Summary:

High Speed:

FPGA Bank 113, Bank 213:

8 GTP channels (4/4) connected to DP pairs

Low Speed:

FPGA Bank 12, Bank 13, Bank 14:

- 34 differential LA pairs
  LA00_CC assigned to bank 13 SRCC port
  LA01_CC assigned to bank 13 MRCC port
  LA17_CC assigned to bank 12 MRCC port
  LA18_CC assigned to bank 12 SRCC port
- 24 differential HA pairs
  HA00_CC assigned to bank 14 SRCC port
  HA01_CC assigned to bank 14 SRCC port
  HA17_CC assigned to bank 14 MRCC port
  HA18_CC assigned to bank 12 SRCC port

Table 7-5 FMC 1 (J18) to FPGA Pinout

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
		A		B		
		GND	1	CLK_DIR	V24	14/IO0**
213/MGTPRX	AJ21	DP1_M2C_P	2	GND		
213/MGTPRX	AK21	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	-	
		GND	5	DP9_M2C_N	-	
213/MGTPRX	AL20	DP2_M2C_P	6	GND		
213/MGTPRX	AM20	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	-	
		GND	9	DP8_M2C_N	-	
213/MGTPRX	AL18	DP3_M2C_P	10	GND		
213/MGTPRX	AM18	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	AJ17	113/MGTPRX0
		GND	13	DP7_M2C_N	AK17	113/MGTPRX0
113/MGTPRX1	AL16	DP4_M2C_P	14	GND		
113/MGTPRX1	AM16	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AJ15	113/MGTPRX2
		GND	17	DP6_M2C_N	AK15	113/MGTPRX2
113/MGTPRX3	AJ13	DP5_M2C_P	18	GND		
113/MGTPRX3	AK13	DP5_M2C_N	19	GND		
		GND	20	GBTCLK1_M2C_P	AG14	113/MGTREF0
		GND	21	GBTCLK1_M2C_N	AH14	113/MGTREF0
213/MGTPTX3	AN23	DP1_C2M_P	22	GND		
213/MGTPTX3	AP23	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	-	
		GND	25	DP9_C2M_N	-	
213/MGTPTX2	AL22	DP2_C2M_P	26	GND		
213/MGTPTX2	AM22	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	-	
		GND	29	DP8_C2M_N	-	
213/MGTPTX0	AN19	DP3_C2M_P	30	GND		
213/MGTPTX0	AP19	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	AN17	113/MGTPTX0
		GND	33	DP7_C2M_N	AP17	113/MGTPTX0
113/MGTPTX1	AN15	DP4_C2M_P	34	GND		
113/MGTPTX1	AP15	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AL14	113/MGTPTX2
		GND	37	DP6_C2M_N	AM14	113/MGTPTX2
113/MGTPTX3	AN13	DP5_C2M_P	38	GND		
113/MGTPTX3	AP13	DP5_C2M_N	39	GND		
		GND	40	RES0	-	
		C		D		
		GND	1	PG_C2M		
213/MGTPTX1	AN21	DP0_C2M_P	2	GND		
213/MGTPTX1	AP21	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	AG20	213/MGTREF0
		GND	5	GBTCLK0_M2C_N	AH20	213/MGTREF0

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
213/MGTPRX	AJ19	DP0_M2C_P	6	GND		
213/MGTPRX	AK19	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AG29	13/IOL12P
		GND	9	LA01_N_CC	AG30	13/IOL12N
13/IOL03P	AH33	LA06_P	10	GND		
13/IOL03N	AH34	LA06_N	11	LA05_P	AG32	13/IOL05P
		GND	12	LA05_N	AH32	13/IOL05N
		GND	13	GND		
13/IOL18P	AE27	LA10_P	14	LA09_P	AG31	13/IOL10P
13/IOL18N	AF27	LA10_N	15	LA09_N	AH31	13/IOL10N
		GND	16	GND		
		GND	17	LA13_P	AG26	13/IOL19P
13/IOL09P	AD28	LA14_P	18	LA13_N	AH26	13/IOL19N
13/IOL09N	AD29	LA14_N	19	GND		
		GND	20	LA17_P_CC	AL30	12/IOL12P
		GND	21	LA17_N_CC	AM30	12/IOL12N
12/IOL11P	AJ29	LA18_P_CC	22	GND		
12/IOL11N	AK30	LA18_N_CC	23	LA23_P	AJ30	12/IOL09P
		GND	24	LA23_N	AK31	12/IOL09N
		GND	25	GND		
12/IOL04P	AK33	LA27_P	26	LA26_P	AL34	12/IOL01P
12/IOL04N	AL33	LA27_N	27	LA26_N	AM34	12/IOL01N
		GND	28	GND		
		GND	29	TCK	-	
35/IOL24N	T9	SCL	30	TDI	-	
35/IOL24P	U9	SDA	31	TDO	-	
		GND	32	3P3VAUX	-	
		GND	33	TMS	-	
	GND	GA0	34	TRST_L	-	
	-	12P0V	35	GA1	GND	
		GND	36	3P3V	-	
	-	12P0V	37	GND		
		GND	38	3P3V	-	
	-	3P3V	39	GND		
		GND	40	3P3V	-	
		E		F		
		GND	1	PG_M2C	AF34	13/IOL01P**
14/IOL14P	AB31	HA01_P_CC	2	GND		
14/IOL14N	AB32	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	W30	14/IOL11P
		GND	5	HA00_N_CC	W31	14/IOL11N
14/IOL09P	V33	HA05_P	6	GND		
14/IOL09N	V34	HA05_N	7	HA04_P	W33	14/IOL08P
		GND	8	HA04_N	W34	14/IOL08N
14/IOL16P	AA32	HA09_P	9	GND		
14/IOL16N	AA33	HA09_N	10	HA08_P	AA34	14/IOL18P
		GND	11	HA08_N	AB34	14/IOL18N
14/IOL17P	AC31	HA13_P	12	GND		
14/IOL17N	AC32	HA13_N	13	HA12_P	AA29	14/IOL22P

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
		GND	14	HA12_N	AB29	14/IOL22N
14/IOL21P	AB26	HA16_P	15	GND		
14/IOL21N	AB27	HA16_N	16	HA15_P	AA27	14/IOL20P
		GND	17	HA15_N	AA28	14/IOL20N
13/IOL23P	AF25	HA20_P	18	GND		
13/IOL23N	AG25	HA20_N	19	HA19_P	AG24	13/IOL21P
		GND	20	HA19_N	AH24	13/IOL21N
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	VADJ	39	GND		
		GND	40	VADJ	-	
		G		H		
		GND	1	VREF_A_M2C	-	
12/IOL13P	AL28	CLK1_M2C_P	2	PRSNT_M2C_L	AD25	13/IOL24P**
12/IOL13N	AL29	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AH28	13/IOL13P
		GND	5	CLK0_M2C_N	AH29	13/IOL13N
13/IOL11P	AF29	LA00_P_CC	6	GND		
13/IOL11N	AF30	LA00_N_CC	7	LA02_P	AD33	13/IOL02P
		GND	8	LA02_N	AD34	13/IOL02N
13/IOL04P	AE33	LA03_P	9	GND		
13/IOL04N	AF33	LA03_N	10	LA04_P	AE32	13/IOL06P
		GND	11	LA04_N	AF32	13/IOL06N
13/IOL07P	AD31	LA08_P	12	GND		
13/IOL07N	AE31	LA08_N	13	LA07_P	AD30	13/IOL08P
		GND	14	LA07_N	AE30	13/IOL08N
13/IOL15P	AD26	LA12_P	15	GND		
13/IOL15N	AE26	LA12_N	16	LA11_P	AG27	13/IOL17P
		GND	17	LA11_N	AH27	13/IOL17N
13/IOL16P	AC26	LA16_P	18	GND		
13/IOL16N	AC27	LA16_N	19	LA15_P	AE23	13/IOL20P
		GND	20	LA15_N	AF23	13/IOL20N
12/IOL02P	AJ33	LA20_P	21	GND		

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
12/IOL02N	AJ34	LA20_N	22	LA19_P	AJ31	12/IOL07P
		GND	23	LA19_N	AK32	12/IOL07N
12/IOL06P	AL32	LA22_P	24	GND		
12/IOL06N	AM32	LA22_N	25	LA21_P	AJ25	12/IOL19P
		GND	26	LA21_N	AK25	12/IOL19N
12/IOL03P	AN34	LA25_P	27	GND		
12/IOL03N	AP34	LA25_N	28	LA24_P	AN31	12/IOL10P
		GND	29	LA24_N	AP31	12/IOL10N
12/IOL05P	AN33	LA29_P	30	GND		
12/IOL05N	AP33	LA29_N	31	LA28_P	AM31	12/IOL08P
		GND	32	LA28_N	AN32	12/IOL08N
12/IOL16P	AM29	LA31_P	33	GND		
12/IOL16N	AN29	LA31_N	34	LA30_P	AP29	12/IOL15P
		GND	35	LA30_N	AP30	12/IOL15N
12/IOL17P	AN28	LA33_P	36	GND		
12/IOL17N	AP28	LA33_N	37	LA32_P	AK27	12/IOL18P
		GND	38	LA32_N	AL27	12/IOL18N
	-	VADJ	39	GND		
		GND	40	VADJ	-	
		J		K		
		GND	1	VREF_B_M2C	-	
13/IOL14P	AE28	CLK3_BIDIR_P	2	GND		
13/IOL14N	AF28	CLK3_BIDIR_N	3	GND		
		GND	4	CLK2_BIDIR_P	Y30	14/IOL12P
		GND	5	CLK2_BIDIR_N	Y31	14/IOL12N
14/IOL07P	V31	HA03_P	6	GND		
14/IOL07N	V32	HA03_N	7	HA02_P	W25	14/IOL05P
		GND	8	HA02_N	Y25	14/IOL05N
14/IOL15P	AC33	HA07_P	9	GND		
14/IOL15N	AC34	HA07_N	10	HA06_P	Y32	14/IOL10P
		GND	11	HA06_N	Y33	14/IOL10N
14/IOL19P	AC28	HA11_P	12	GND		
14/IOL19N	AC29	HA11_N	13	HA10_P	AA24	14/IOL23P
		GND	14	HA10_N	AA25	14/IOL23N
14/IOL24P	AB24	HA14_P	15	GND		
14/IOL24N	AB25	HA14_N	16	HA17_P_CC	AA30	14/IOL13P
		GND	17	HA17_N_CC	AB30	14/IOL13N
12/IOL14P	AJ28	HA18_CC_P	18	GND		
12/IOL14N	AK28	HA18_CC_N	19	HA21_P	AC24	13/IOL22P
		GND	20	HA21_N	AD24	13/IOL22N
12/IOL20P	AJ26	HA22_P	21	GND		
12/IOL20N	AK26	HA22_N	22	HA23_P	AM26	12/IOL21P
		GND	23	HA23_N	AN26	12/IOL21N
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
	-	HB11_P	30	GND		
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	VIO_B_M2C	39	GND		
		GND	40	VIO_B_M2C	-	

**Note: CLK DIR, PRSNT, PG are all inverted before application to FPGA IO

7.5.2. FMC HPC 2 (J19) IO Allocation

This FMC connects all 34 LAxx differential pairs and 12 HAxx differential pairs to banks on the FPGA. HBxx ports are not connected. Eight high-speed DP lanes are provisioned with GTP pairs (TX and RX) and both GBT Clocks are received.

Quick Summary:

High Speed:

FPGA Bank 116, Bank 216:

8 GTP channels (4/4) connected to DP pairs

Low Speed:

FPGA Bank 15, Bank 16

- 34 differential LA pairs
  LA00_CC assigned to bank 15 MRCC port
  LA01_CC assigned to bank 15 SRCC port
  LA17_CC assigned to bank 16 SRCC port
  LA18_CC assigned to bank 16 MRCC port

- 12 differential HA pairs
  HA00_CC assigned to bank 15 SRCC port
  HA01_CC assigned to bank 16 SRCC port

Table 7-6 FMC 2 (J19) to FPGA Pinout

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
		A		B		
		GND	1	CLK_DIR		
116/MGTP	F13	DP1_M2C_P	2	GND		
116/MGTP	E13	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P		
		GND	5	DP9_M2C_N		
116/MGTP	D16	DP2_M2C_P	6	GND		
116/MGTP	C16	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P		
		GND	9	DP8_M2C_N		
116/MGTP	F17	DP3_M2C_P	10	GND		
116/MGTP	E17	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	D18	216/MGTPRX3
		GND	13	DP7_M2C_N	C18	216/MGTPRX3
216/MGTP	F19	DP4_M2C_P	14	GND		
216/MGTP	E19	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	D20	216/MGTPRX1
		GND	17	DP6_M2C_N	C20	216/MGTPRX1
216/MGTP	F21	DP5_M2C_P	18	GND		
216/MGTP	E21	DP5_M2C_N	19	GND		
		GND	20	GBTCLK1_M2C_P	H18	216/MGTREF0
		GND	21	GBTCLK1_M2C_N	G18	216/MGTREF0
116/MGTPT	B13	DP1_C2M_P	22	GND		
116/MGTPT	A13	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P		
		GND	25	DP9_C2M_N		
116/MGTPT	B15	DP2_C2M_P	26	GND		
116/MGTPT	A15	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P		
		GND	29	DP8_C2M_N		
116/MGTPT	B17	DP3_C2M_P	30	GND		
116/MGTPT	A17	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	B19	216/MGTPTX3
		GND	33	DP7_C2M_N	A19	216/MGTPTX3
216/MGTP	B21	DP4_C2M_P	34	GND		
216/MGTP	A21	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	D22	216/MGTPTX1
		GND	37	DP6_C2M_N	C22	216/MGTPTX1
216/MGTP	B23	DP5_C2M_P	38	GND		
216/MGTP	A23	DP5_C2M_N	39	GND		
		GND	40	RES0	-	
		C		D		
		GND	1	PG_C2M		
116/MGTPT	D14	DP0_C2M_P	2	GND		
116/MGTPT	C14	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	H16	116/MGTREF0
		GND	5	GBTCLK0_M2C_N	G16	116/MGTREF0
116/MGTP	F15	DP0_M2C_P	6	GND		

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
116/MGTP	E15	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	U29	15/IOL11P
		GND	9	LA01_N_CC	T29	15/IOL11N
15/IOL05P	U26	LA06_P	10	GND		
15/IOL05N	U27	LA06_N	11	LA05_P	U25	15/IOL03P
		GND	12	LA05_N	T25	15/IOL03N
		GND	13	GND		
15/IOL06P	R25	LA10_P	14	LA09_P	N26	15/IOL02P
15/IOL06N	P25	LA10_N	15	LA09_N	M27	15/IOL02N
		GND	16	GND		
		GND	17	LA13_P	N29	15/IOL10P
15/IOL15P	M30	LA14_P	18	LA13_N	M29	15/IOL10N
15/IOL15N	M31	LA14_N	19	GND		
		GND	20	LA17_P_CC	L28	16/IOL11P
		GND	21	LA17_N_CC	K28	16/IOL11N
16/IOL12P	J28	LA18_P_CC	22	GND		
16/IOL12N	H28	LA18_N_CC	23	LA23_P	M25	16/IOL05P
		GND	24	LA23_N	L25	16/IOL05N
		GND	25	GND		
16/IOL02P	K23	LA27_P	26	LA26_P	J24	16/IOL06P
16/IOL02N	J23	LA27_N	27	LA26_N	H24	16/IOL06N
		GND	28	GND		
		GND	29	TCK	-	
35/IOL24N	T9	SCL	30	TDI	-	
35/IOL24P	U9	SDA	31	TDO	-	
		GND	32	3P3VAUX	-	
		GND	33	TMS	-	
	GND	GA0	34	TRST_L	-	
	-	12P0V	35	GA1	3.3V***	
		GND	36	3P3V	-	
	-	12P0V	37	GND		
		GND	38	3P3V	-	
	-	3P3V	39	GND		
		GND	40	3P3V	-	
		E		F		
		GND	1	PG_M2C	AG34	13/IOL01N**
16/IOL14P	K30	HA01_P_CC	2	GND		
16/IOL14N	J30	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	U30	15/IOL14P
		GND	5	HA00_N_CC	T30	15/IOL14N
15/IOL20P	N32	HA05_P	6	GND		
15/IOL20N	N33	HA05_N	7	HA04_P	N34	15/IOL22P
		GND	8	HA04_N	M34	15/IOL22N
16/IOL22P	L32	HA09_P	9	GND		
16/IOL22N	K32	HA09_N	10	HA08_P	K33	16/IOL20P
		GND	11	HA08_N	J34	16/IOL20N
	-	HA13_P	12	GND		
	-	HA13_N	13	HA12_P	-	
		GND	14	HA12_N	-	

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
	-	HA16_P	15	GND		
	-	HA16_N	16	HA15_P	-	
		GND	17	HA15_N	-	
	-	HA20_P	18	GND		
	-	HA20_N	19	HA19_P	-	
		GND	20	HA19_N	-	
	-	HB03_P	21	GND		
	-	HB03_N	22	HB02_P	-	
		GND	23	HB02_N	-	
	-	HB05_P	24	GND		
	-	HB05_N	25	HB04_P	-	
		GND	26	HB04_N	-	
	-	HB09_P	27	GND		
	-	HB09_N	28	HB08_P	-	
		GND	29	HB08_N	-	
	-	HB13_P	30	GND		
	-	HB13_N	31	HB12_P	-	
		GND	32	HB12_N	-	
	-	HB19_P	33	GND		
	-	HB19_N	34	HB16_P	-	
		GND	35	HB16_N	-	
	-	HB21_P	36	GND		
	-	HB21_N	37	HB20_P	-	
		GND	38	HB20_N	-	
	-	VADJ	39	GND		
		GND	40	VADJ	-	
		G		H		
		GND	1	VREF_A_M2C	-	
16/IOL13P	J29	CLK1_M2C_P	2	PRSNT_M2C_L	AE25	13/IOL24N**
16/IOL13N	H29	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	R30	15/IOL13P
		GND	5	CLK0_M2C_N	P30	15/IOL13N
15/IOL12P	P28	LA00_P_CC	6	GND		
15/IOL12N	P29	LA00_N_CC	7	LA02_P	P24	15/IOL04P
		GND	8	LA02_N	N24	15/IOL04N
15/IOL09P	T28	LA03_P	9	GND		
15/IOL09N	R28	LA03_N	10	LA04_P	T27	15/IOL07P
		GND	11	LA04_N	R27	15/IOL07N
15/IOL08P	N27	LA08_P	12	GND		
15/IOL08N	N28	LA08_N	13	LA07_P	U31	15/IOL18P
		GND	14	LA07_N	U32	15/IOL18N
15/IOL17P	N31	LA12_P	15	GND		
15/IOL17N	M32	LA12_N	16	LA11_P	T32	15/IOL19P
		GND	17	LA11_N	R32	15/IOL19N
15/IOL01P	R26	LA16_P	18	GND		
15/IOL01N	P26	LA16_N	19	LA15_P	R31	15/IOL16P
		GND	20	LA15_N	P31	15/IOL16N
16/IOL01P	M24	LA20_P	21	GND		
16/IOL01N	L24	LA20_N	22	LA19_P	K25	16/IOL04P

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
		GND	23	LA19_N	J25	16/IOL04N
16/IOL10P	K26	LA22_P	24	GND		
16/IOL10N	J26	LA22_N	25	LA21_P	G29	16/IOL15P
		GND	26	LA21_N	G30	16/IOL15N
16/IOL03P	G24	LA25_P	27	GND		
16/IOL03N	G25	LA25_N	28	LA24_P	L27	16/IOL09P
		GND	29	LA24_N	K27	16/IOL09N
16/IOL08P	H26	LA29_P	30	GND		
16/IOL08N	G26	LA29_N	31	LA28_P	H27	16/IOL07P
		GND	32	LA28_N	G27	16/IOL07N
16/IOL17P	H31	LA31_P	33	GND		
16/IOL17N	G31	LA31_N	34	LA30_P	H32	16/IOL19P
		GND	35	LA30_N	G32	16/IOL19N
16/IOL16P	K31	LA33_P	36	GND		
16/IOL16N	J31	LA33_N	37	LA32_P	L29	16/IOL18P
		GND	38	LA32_N	L30	16/IOL18N
	-	VADJ	39	GND		
		GND	40	VADJ	-	
		J		K		
		GND	1	VREF_B_M2C	-	
	-	CLK3_BIDIR_P	2	GND		
	-	CLK3_BIDIR_N	3	GND		
		GND	4	CLK2_BIDIR_P	-	
		GND	5	CLK2_BIDIR_N	-	
15/IOL24P	P33	HA03_P	6	GND		
15/IOL24N	P34	HA03_N	7	HA02_P	U34	15/IOL23P
		GND	8	HA02_N	T34	15/IOL23N
16/IOL23P	J33	HA07_P	9	GND		
16/IOL23N	H34	HA07_N	10	HA06_P	T33	15/IOL21P
		GND	11	HA06_N	R33	15/IOL21N
16/IOL21P	H33	HA11_P	12	GND		
16/IOL21N	G34	HA11_N	13	HA10_P	L33	16/IOL24P
		GND	14	HA10_N	L34	16/IOL24N
	-	HA14_P	15	GND		
	-	HA14_N	16	HA17_P_CC	-	
		GND	17	HA17_N_CC	-	
	-	HA18_P	18	GND		
	-	HA18_N	19	HA21_P	-	
		GND	20	HA21_N	-	
	-	HA22_P	21	GND		
	-	HA22_N	22	HA23_P	-	
		GND	23	HA23_N	-	
	-	HB01_P	24	GND		
	-	HB01_N	25	HB00_P_CC	-	
		GND	26	HB00_N_CC	-	
	-	HB07_P	27	GND		
	-	HB07_N	28	HB06_P_CC	-	
		GND	29	HB06_N_CC	-	
	-	HB11_P	30	GND		

BANK/IO #	PIN #	FMC PIN NAME			PIN #	BANK/IO #
	-	HB11_N	31	HB10_P	-	
		GND	32	HB10_N	-	
	-	HB15_P	33	GND		
	-	HB15_N	34	HB14_P	-	
		GND	35	HB14_N	-	
	-	HB18_P	36	GND		
	-	HB18_N	37	HB17_P_CC	-	
		GND	38	HB17_N_CC	-	
	-	VIO_B_M2C	39	GND		
		GND	40	VIO_B_M2C	-	

**Note: PRSNT and PG signal are inverted before it is applied to FPGA IO

***Note: As the two FMCs share a single I2C bus, FMC 2 is set for a higher I2C slave address.

7.6. DDR3 SDRAM SODIMM Connector

The TB-A7-200T-IMG development board includes a JEDEC standard 204-pin DDR3 SODIMM receptacle that can accept a DDR3 SDRAM module. Since the Data lines originate at FPGA SelectIO pins, the -2 speed grade device on this board can support up to 800MT/s (400MHz Clock) in a 64-bit controller structure (see Xilinx datasheet “DS181: Artix-7 FPGAs DC and Switching Characteristics”). The clock generator CLK1 output generates the clock timing for the DDR3 controller through SYSCLK, and can be set anywhere between 200-400MHz depending on the SDRAM speed grade.

DDR3 SDRAM SODIMM

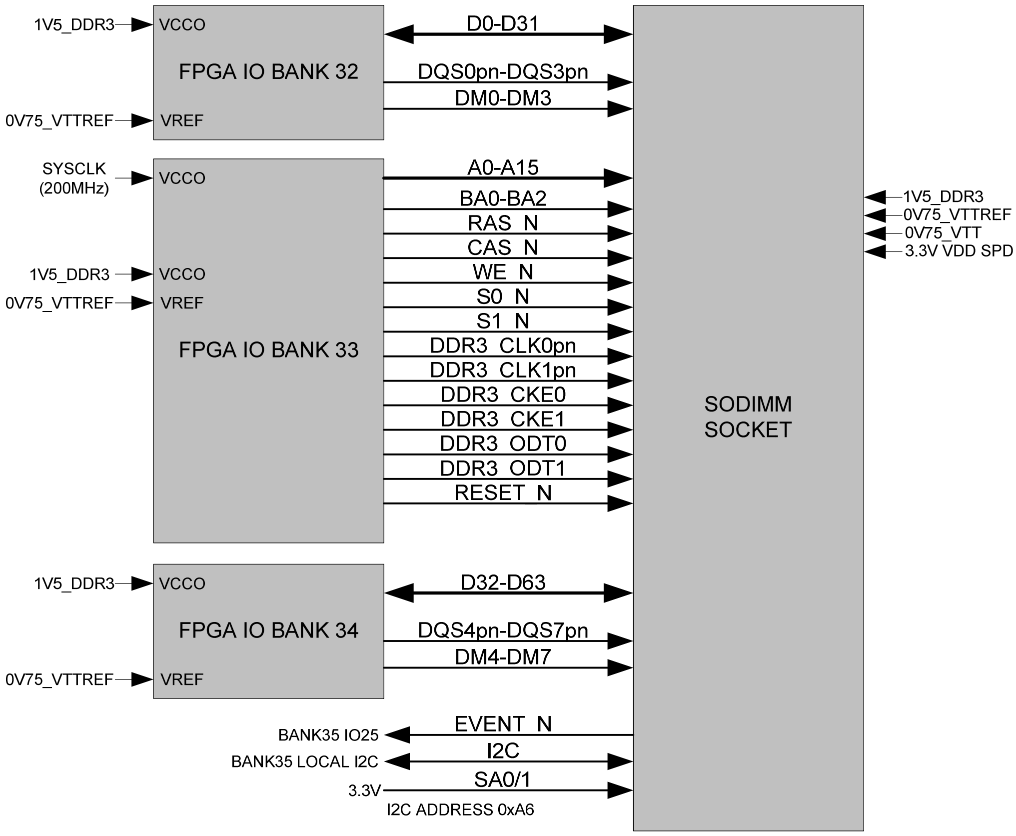


Figure 7-13 DDR3 SDRAM SODIMM Structure

The DDR3 bank arrangement, DQS IO assignments, clock connections, and Vref provisions follow the suggested memory structure in Xilinx document “UG586: Zynq-7000 All Programmable SoC and 7 Series Devices Memory Interface Solutions User Guide”. Using features built into the Vivado Suite, a DDR3 memory controller can be readily and easily generated following the procedure described in Chapter 1. The following table group provides the Pin IO mapping of the DDR3 Banks to the SODIMM module:

Table 7-7 FPGA IO PINOUT MAPPING TO SODIMM SOCKET

No.	SODIMM PIN NAME	SODIMM PIN NUMBER	FPGA BANK_ PIN FUNCTION	FPGA PIN NUMBER
1	A0	98	B33_IO/L5_P/T0	AF3
2	A1	97	B33_IO/L1_P/T0	AG1
3	A2	96	B33_IO/L9_P/T1/DQS_P	AH4
4	A3	95	B33_IO/L5_N/T0	AG2
5	A4	92	B33_IO/L7_N/T1	AG4
6	A5	91	B33_IO/L1_N/T0	AH1
7	A6	90	B33_IO/L17_N/T2	AH6
8	A7	86	B33_IO/L17_P/T2	AH7
9	A8	89	B33_IO/L3_P/T0/DQS_P	AH2
10	A9	85	B33_IO/L3_N/T0/DQS_N	AJ1
11	A10/AP	107	B33_IO/L2_N/T0	AE1
12	A11	84	B33_IO/L14_P/T2/SRCC	AF7
13	A12/BC_N	83	B33_IO/L6_P/T0	AH3
14	A13	119	B33_IO/L10_P/T1	AD3
15	A14	80	B33_IO/L14_N/T2/SRCC	AG7
16	A15	78	B33_IO/L18_P/T2	AF9
17	BA0	109	B33_IO/L4_N/T0	AF2
18	BA1	108	B33_IO/L8_N/T1	AD4
19	BA2	79	B33_IO/L7_P/T1	AF4
20	RAS_N	110	B33_IO/L8_P/T1	AD5
21	CAS_N	115	B33_IO/L4_P/T0	AE2
22	WE_N	113	B33_IO/L2_P/T0	AD1
23	CLK0_P	101	B33_IO/L11_P/T1/SRCC	AG6
24	CLK0_N	103	B33_IO/L11_N/T1/SRCC	AG5
25	CLK1_P	102	B33_IO/L12_P/T1/MRCC	AE5
26	CLK1_N	104	B33_IO/L12_N/T1/MRCC	AF5
27	CKE0	73	B33_IO/L9_N/T1/DQS_N	AJ4
28	CKE1	74	B33_IO/L16_P/T2	AE8
29	ODT0	116	B33_IO/L15_N/T2/DQS_N	AD8
30	ODT1	120	B33_IO/L15_P/T2/DQS_P	AD9
31	RESET_N	30	B33_IO/0	AC11
32	S0_N	114	B33_IO/L16_N/T2	AE7
33	S1_N	121	B33_IO/L10_N/T1	AE3
34	DQ0	5	B32_IO/L1_P/T0	AN1
35	DQ1	7	B32_IO/L1_N/T0	AP1
36	DQ2	15	B32_IO/L2_P/T0	AK2
37	DQ3	17	B32_IO/L2_N/T0	AK1
38	DQ4	4	B32_IO/L4_P/T0	AL2
39	DQ5	6	B32_IO/L4_N/T0	AM1
40	DQ6	16	B32_IO/L5_P/T0	AN3
41	DQ7	18	B32_IO/L5_N/T0	AP3

No.	SODIMM PIN NAME	SODIMM PIN NUMBER	FPGA BANK_ PIN FUNCTION	FPGA PIN NUMBER
42	DQ8	21	B32_IO/L7_P/T1	AN4
43	DQ9	23	B32_IO/L7_N/T1	AP4
44	DQ10	33	B32_IO/L8_P/T1	AJ5
45	DQ11	35	B32_IO/L8_N/T1	AK5
46	DQ12	22	B32_IO/L10_P/T1	AL4
47	DQ13	24	B32_IO/L10_N/T1	AM4
48	DQ14	34	B32_IO/L11_P/T1/SRCC	AL5
49	DQ15	36	B32_IO/L11_N/T1/SRCC	AM5
50	DQ16	39	B32_IO/L13_P/T2/MRCC	AK7
51	DQ17	41	B32_IO/L13_N/T2/MRCC	AL7
52	DQ18	51	B32_IO/L14_P/T2/SRCC	AM7
53	DQ19	53	B32_IO/L14_N/T2/SRCC	AM6
54	DQ20	40	B32_IO/L16_P/T2	AN8
55	DQ21	42	B32_IO/L16_N/T2	AP8
56	DQ22	50	B32_IO/L17_P/T2	AN7
57	DQ23	52	B32_IO/L17_N/T2	AN6
58	DQ24	57	B32_IO/L19_P/T3	AJ10
59	DQ25	59	B32_IO/L20_P/T3	AP11
60	DQ26	67	B32_IO/L20_N/T3	AP10
61	DQ27	69	B32_IO/L22_P/T3	AM11
62	DQ28	56	B32_IO/L22_N/T3	AN11
63	DQ29	58	B32_IO/L23_P/T3	AJ11
64	DQ30	68	B32_IO/L23_N/T3	AK11
65	DQ31	70	B32_IO/L24_P/T3	AL10
66	DQ32	129	B34_IO/L1_P/T0	W10
67	DQ33	131	B34_IO/L1_N/T0	Y10
68	DQ34	141	B34_IO/L2_P/T0	V9
69	DQ35	143	B34_IO/L2_N/T0	V8
70	DQ36	130	B34_IO/L4_P/T0	V7
71	DQ37	132	B34_IO/L4_N/T0	V6
72	DQ38	140	B34_IO/L5_P/T0	Y8
73	DQ39	142	B34_IO/L5_N/T0	Y7
74	DQ40	147	B34_IO/L7_P/T1	W1
75	DQ41	149	B34_IO/L7_N/T1	Y1
76	DQ42	157	B34_IO/L8_P/T1	V2
77	DQ43	159	B34_IO/L8_N/T1	V1
78	DQ44	146	B34_IO/L10_P/T1	V3
79	DQ45	148	B34_IO/L10_N/T1	W3
80	DQ46	158	B34_IO/L11_P/T1/SRCC	V4
81	DQ47	160	B34_IO/L11_N/T1/SRCC	W4
82	DQ48	163	B34_IO/L13_P/T2/MRCC	AA5
83	DQ49	165	B34_IO/L13_N/T2/MRCC	AA4
84	DQ50	175	B34_IO/L14_P/T2/SRCC	AB5

No.	SODIMM PIN NAME	SODIMM PIN NUMBER	FPGA BANK_ PIN FUNCTION	FPGA PIN NUMBER
85	DQ51	177	B34_IO/L14_N/T2/SRCC	AB4
86	DQ52	164	B34_IO/L16_P/T2	AA3
87	DQ53	166	B34_IO/L16_N/T2	AA2
88	DQ54	174	B34_IO/L17_P/T2	AC2
89	DQ55	176	B34_IO/L17_N/T2	AC1
90	DQ56	181	B34_IO/L19_P/T3	AA8
91	DQ57	183	B34_IO/L20_P/T3	AC7
92	DQ58	191	B34_IO/L20_N/T3	AC6
93	DQ59	193	B34_IO/L22_P/T3	AC9
94	DQ60	180	B34_IO/L22_N/T3	AC8
95	DQ61	182	B34_IO/L23_P/T3	AA10
96	DQ62	192	B34_IO/L23_N/T3	AA9
97	DQ63	194	B34_IO/L24_P/T3	AB10
98	DM0	11	B32_IO/L6_P/T0	AK3
99	DM1	28	B32_IO/L12_P/T1/MRCC	AJ6
100	DM2	46	B32_IO/L18_P/T2	AN9
101	DM3	63	B32_IO/L24_N/T3	AM10
102	DM4	136	B34_IO/L6_P/T0	W6
103	DM5	153	B34_IO/L12_P/T1/MRCC	W5
104	DM6	170	B34_IO/L18_P/T2	AC4
105	DM7	187	B34_IO/L24_N/T3	AB9
106	DQS0_P	12	B32_IO/L3_P/T0/DQS_P	AM2
107	DQS0_N	10	B32_IO/L3_N/T0/DQS_N	AN2
108	DQS1_P	29	B32_IO/L9_P/T1/DQS_P	AP6
109	DQS1_N	27	B32_IO/L9_N/T1/DQS_N	AP5
110	DQS2_P	47	B32_IO/L15_P/T2/DQS_P	AJ8
111	DQS2_N	45	B32_IO/L15_N/T2/DQS_N	AK8
112	DQS3_P	64	B32_IO/L21_P/T3/DQS_P	AL9
113	DQS3_N	62	B32_IO/L21_N/T3/DQS_N	AM9
114	DQS4_P	137	B34_IO/L3_P/T0/DQS_P	W9
115	DQS4_N	135	B34_IO/L3_N/T0/DQS_N	W8
116	DQS5_P	154	B34_IO/L9_P/T1/DQS_P	Y3
117	DQS5_N	152	B34_IO/L9_N/T1/DQS_N	Y2
118	DQS6_P	171	B34_IO/L15_P/T2/DQS_P	AB2
119	DQS6_N	169	B34_IO/L15_N/T2/DQS_N	AB1
120	DQS7_P	188	B34_IO/L21_P/T3/DQS_P	AB7
121	DQS7_N	186	B34_IO/L21_N/T3/DQS_N	AB6
122	EVENT_N	198	B35_IO/25	U11

7.7. Ethernet 100/1000 Interface

The TB-A7-200T-IMG contains a 100/1000 Ethernet PHY and RJ45 jack that can accept a standard Ethernet twisted-pair cable. The PHY is a Marvell Alaska® 88E1116R Gigabit Ethernet Transceiver that features: Auto-MDI/MDIX, integrated loopback capability, programmable LED functions, and multi IO-standard RGMII interface. The following table details the PHY RGMII pin interconnection to FPGA Bank 36 pins:

Table 7-8 Ethernet PHY FPGA Pin Assignment

PHY pin name	PHY pin #	Signal Name	FPGA Bank 36 IO function	FPGA Pin
MDC	48	CLK_PHY_MDC	IO/L19_N/T3/VREF	L3
RX_CLK	53	CLK_PHY_RX_CLK	IO/L13_P/T2/MRCC	G5
TX_CLK	60	CLK_PHY_TX_CLK	IO/L12_P/T1/MRCC	H7
MDIO	45	PHY_MDIO_OD	IO/L20_P/T3	H2
RESET_N	10	PHY_RESET_N	IO/L19_P/T3	L4
RX_CTRL	49	PHY_RX_CTRL	IO/L23_N/T3	L2
RXD0	50	PHY_RXD0	IO/L23_P/T3	M2
RXD1	51	PHY_RXD1	IO/L24_P/T3	K3
RXD2	54	PHY_RXD2	IO/L24_N/T3	K2
RXD3	55	PHY_RXD3	IO/25	L7
TX_CTRL	63	PHY_TX_CTRL	IO/L20_N/T3	G2
TXD0	58	PHY_TXD0	IO/L21_P/T3/DQS_P	K1
TXD1	59	PHY_TXD1	IO/L21_N/T3/DQS_N	J1
TXD2	61	PHY_TXD2	IO/L22_P/T3	H1
TXD3	62	PHY_TXD3	IO/L22_N/T3	G1

The PHY has a 25MHz crystal oscillator from which it derives all its line interface timing. The RX CLK and TX CLK signals on the MRCC FPGA pins can operate at up to 125MHz for Gigabit line rate, supporting DDR transfer rates of 250Mb/s per pin on each of the four RGMII pins in each direction. The user is cautioned about relying on these clocks for unrelated circuitry in the FPGA as the frequency is line rate dependent and RX CLK can exhibit disturbances as the line status changes.

The 88E1116R PHY device provides some reset-time configuration options, selected by shunt clips on several 1x3 headers as follows (shorted pin pairs indicated).

Note: Only two shunt clips must be used at a time; one for either J11 or J12, and the other for either J13 or J14 ("N-A" = Not Allowed). Incorrect operation can result in permanent damage to the board.

Table 7-9 Ethernet PHY reset Configuration Selection

Header J11	Header J12	Header J13	Header J14	PHY configuration function
1-2	N-A	x	x	Disable Auto crossover, PHY SMBus address A4=0
N-A	1-2	x	x	Enable Auto crossover, PHY SMBus address A4=1
N-A	2-3	x	x	Disable Auto crossover, PHY SMBus address A4=1
x	x	1-2	N-A	TX CLK Delayed, RX CLK on RXD change
x	x	2-3	N-A	TX CLK no Delay, RX CLK on RXD stable
x	x	N-A	1-2	TX CLK Delayed, RX CLK on RXD stable
x	x	N-A	2-3	TX CLK no Delay, RX CLK on RXD change

Note: PHY SMBus address bits 3-0 are fixed on the PCB at b0111

Ethernet line connection is provided through a Halo HFJ11-1G01ERL shielded integrated-magnetics 8P8C modular jack that contains 4-lane isolating transformers and HV capacitor for the line-side common-mode returns (often called the "Bob Smith Termination"). The Ethernet Status LEDs are mounted on the PCB; LED D23 indicates Link status, D22 indicates line activity, and D21 can be user programmed for any special Ethernet condition indication per the LED options provided by the PHY.

7.8. USB to UART Controller

The TB-A7-200T-IMG features a Silicon Labs CP2103 USB-to-UART interface to communicate with a PC. This module creates a virtual COM port on the computer (driver installation required, refer to silabs.com for PN: CP2103) to allow the user to connect through standard USB. The USB interface on this card is Micro USB **Type AB** which mates with either Micro-A or Micro-B cables.

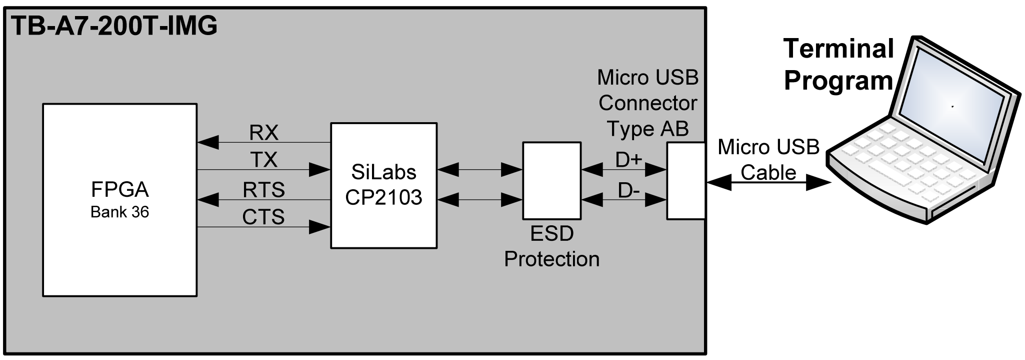
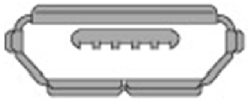
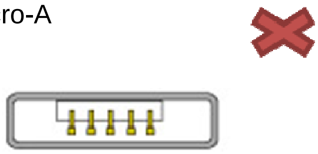
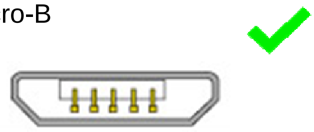
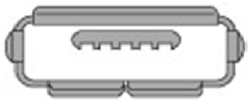
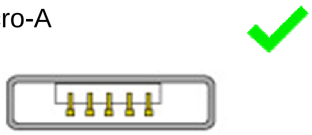
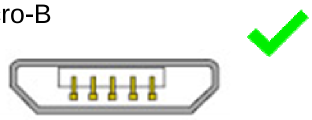


Figure 7-14 USB UART Interface

Table 7-10 Micro-USB Type B and AB Compatibility

Receptacle	Plug
Micro-B 	Micro-A 
	Micro-B 
Micro-AB 	Micro-A 
	Micro-B 

The UART signals are connected to the FPGA's single-ended pins on Bank 36. Provided below is a table indicating where the signals connect. Both the UART transmit and receive data signals are connected as well as flow control signals. Using the PC's virtual COM port drivers, there are different supported baud rates that are compatible with this controller and can be set during the COM port configuration.

Table 7-11 UART Interface FPGA Bank 36 Pin Assignment

USB_UART_TX	USB_UART_RX	USB_UART_RTS_N	USB_UART_CTS_N
H4	H3	J3	J4

7.9. Battery Option

The TB-A7-200T-IMG contains an optional (not populated) LR44 11.6 mm coin cell battery holder connected to the FPGA VBATT pin which serves as a battery backup supply for the FPGA's internal RAM that stores the key for AES decryption. The coin cell, an LR44 1.5V battery (silver oxide or Alkaline cell), provides the memory state retention power required. The holder is not installed and is a factory option; please contact our sales representative if you require this option.

Note that the battery holder outer metal cage connects to the positive pole of the battery and can be used as a probe TP to measure the voltage. A series resistance (not populated) in the negative pole protects the cell from dead shorts, however, avoid touching the holder cage exposed metal with grounded metal objects such as grounded probe clips. At maximum specified FPGA VBAT current, the voltage drop across the protection resistor is 1.5mV.

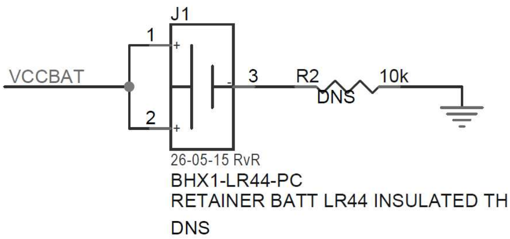


Figure 7-15 Battery Circuit

The maximum battery current specified for the Artix-7 series is 150nA. This calculates to 10^6 hours of backup using common Alkaline LR44 cells with a typical capacity of 150mAhrs, far exceeding the shelf life of the battery. SR44 Silver Oxide cells may also be used, however, they may contain mercury and can become hazardous if leakage develops after long use.

Regardless of battery chemistry, the battery cell should be replaced at timely intervals (3-4yrs max.) to reduce the possibility of leakage which could damage the holder and PCB. Refere to manufacturer's requirements. If any leakage is observed, the battery cell must be immediately removed from the holder using appropriate safe handling procedures. Any leaked material should be cleaned away from the PCB using a suitable board wash solution and the PCB area where leaked material was found closely examined for damage that might impact operation.

7.10. Quad (x4) SPI Flash and FPGA Configuration

The TB-A7-200T-IMG has a single 256Mbit quad SPI flash memory for FPGA configuration and user data storage purposes. Since the XC7A200T consumes 78Mbits of space for configuration, at least 128Mb is available for user data storage. Please refer to "UG470: 7 Series FPGAs Configuration User Guide" for details on the operation of device configuration.

Device: Micron N25Q256A13EF840E 256Mbit, x1/x2/x4 support
Data Rate: 100 MHz (maximum) clock frequency in single transfer rate mode

Access to programming the FPGA configuration image as well as user data store in the Flash has been provided to the Xilinx core through Bank 35 GPIO pins (shown in figure below).

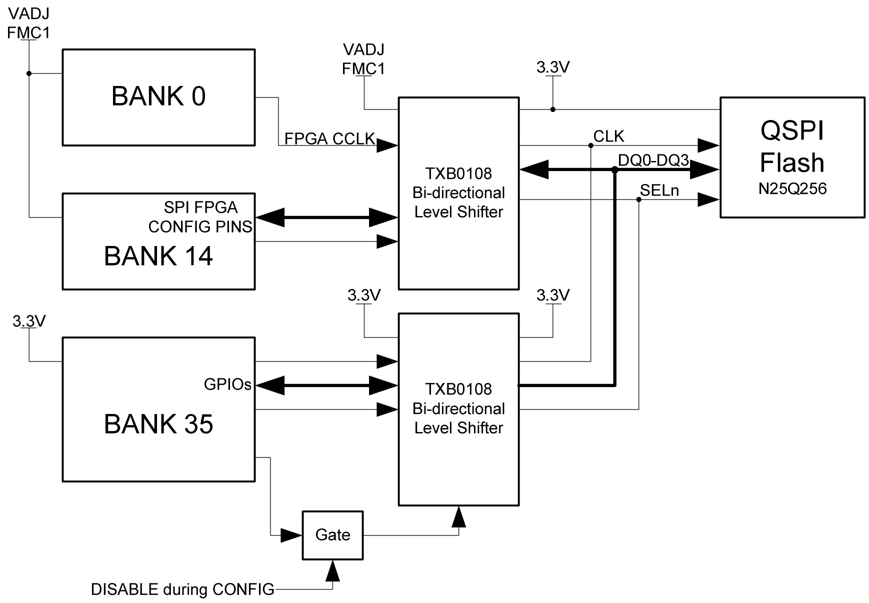


Figure 7-16 FPGA SPI Flash Configuration Structure

The flash may be programmed via JTAG, either through the JTAG header or via the Digilent USB-to-JTAG interface module. The JTAG configuration process uses the FPGA's built-in SPI Flash writing facility in conjunction with Vivado, which requires specific Bank 14 attachment using a supported SPI flash device. Additionally, the FPGA can be configured via SPI or JTAG. JTAG configuration mode is activated by installing a shorting shunt across header pins J26 (standard 2.54mm pitch).

Table 7-12 SPI Flash Memory to FPGA Pin Assignment

Signal Name	FPGA Bank	FPGA Pin Name	FPGA Pin
FPGA Configuration Flash IO			
QSPI_VADJ_CS_N	14	B14_IO/L6_P/T0/FCS_N	Y27
QSPI_VADJ_D0	14	B14_IO/L1_N/T0/D01/DIN	V28
QSPI_VADJ_D1	14	B14_IO/L1_P/T0/D00/MOSI	V29
QSPI_VADJ_D2	14	B14_IO/L2_P/T0/D02	V26
QSPI_VADJ_D3	14	B14_IO/L2_N/T0/D03	V27
CLK_FPGA_CCLK	0	B0_CCLK	W11
Xilinx Flash User IO			
CLK_FPGA_QSPI_C	35	B35_IO/L14_P/T2/SRCC	T5
FPGA_QSPI_D0	35	B35_IO/L9_N/T1/DQS_N/AD7_N	P1
FPGA_QSPI_D1	35	B35_IO/L10_P/T1/AD15_P	N3
FPGA_QSPI_D2	35	B35_IO/L10_N/T1/AD15_N	N2
FPGA_QSPI_D3	35	B35_IO/L11_P/T1/SRCC	P4
FPGA_QSPI_S_N	35	B35_IO/L11_N/T1/SRCC	P3
FPGA_QSPI_OE_N	35	B35_IO/L14_N/T2/SRCC	T4

7.11. EEPROM, 2kbit I2C

An onboard 2kbit I2C EEPROM (M24C02) is programmed with various manufacturing information. The EEPROM is permanently enabled for writing. It is permissible to store custom data in this EEPROM, however, one must be careful to ensure that the manufacturing information is never overwritten.

The contents of the EEPROM are displayed in Appendix A.

Note: The user must be cognizant that the FMC I2C EEPROM is always write-enabled. As it contains critical information, one must never overwrite the factory settings.

7.12. JTAG and Pmod™ Interface

7.12.1. Optional JTAG Connector

The TB-A7-200T-IMG provides an optional JTAG interface that follows the Xilinx 14-pin JTAG standard. The user may connect the Xilinx development system to the board either by Xilinx USB Platform Cable adapter through the JTAG header, or via USB directly through J27 (Micro-USB type A/B) and the Digilent JTAG interface module U55. Stuffing options are provided to allow the Digilent module to control its JTAG bus buffer through a GPIO on the module, or unconditionally enable or disable the buffer.

The JTAG interface has access to the FMC JTAG loop as well, with the FMC data path chained from the FPGA JTAG TDO. Onboard circuitry ensures that the JTAG data path loop is properly closed when only one FMC module is present, automatically shunting JTAG TDI to TDO in any unoccupied FMC slot.

Note: Only one JTAG connection should be used at a time. Either Digilent JTAG or JTAG header. Do not plug into both at the same time.

Table 7-13 J2 Xilinx 14-pin JTAG Pinout

Pin	Xilinx 14-pin JTAG		Pin
1	GND	VREF	2
3	GND	TMS	4
5	GND	TCK	6
7	GND	TDO	8
9	GND	TDI	10
11	GND	NC	12
13	GND	NC	14

Note: VREF is driven by VADJ_FMC1

Table 7-14 FPGA Bank 0 JTAG Pin Assignment

Signal Name	TMS	TCK	TDO	TDI
FPGA Bank 0 Pin	AE13	AE12	AD13	AE14

As mentioned in the SPI Flash section, the FPGA can be directly configured from JTAG. JTAG configuration mode is activated by installing a shorting shunt across header pins J26 (standard 2.54mm pitch).

7.12.2. Pmod™ Interface

The TB-A7-200T-IMG features two Digilent Pmod standard 2.54mm right-angle 2x6 female receptacles for interconnections that include eight bi-directional digital CMOS level I/O signals, 3.3V and ground. These connectors directly support 6 or 12-pin Pmod standard peripheral modules that feature a large number of general and special IO functions.

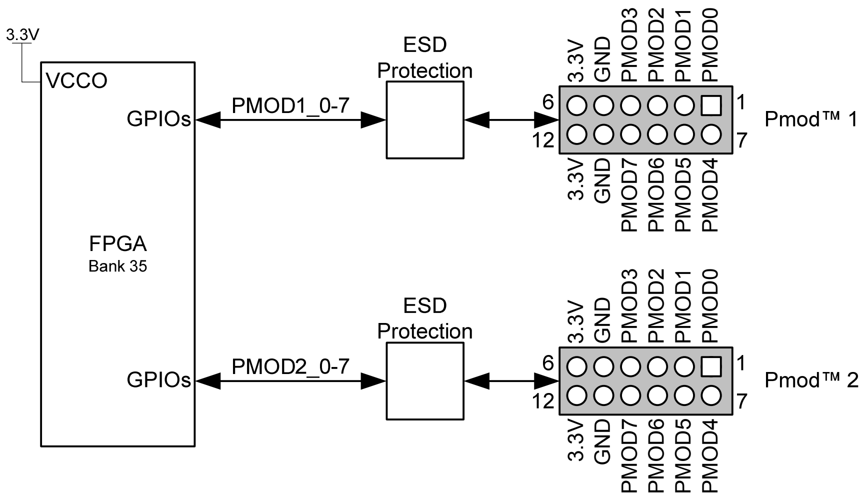


Figure 7-17 Pmod Connections

Since the connector IO pins drive straight from FPGA IOs, protective TVS diode clamping blocks are attached to each group of signals to counter any ESD or surge injection into the connector pins.

The following tables detail the mapping of the two Pmod IO connector pins to FPGA IO pins. There is no series resistance present in the signal lines and the full output drive capability of the FPGA IOs is available. Refer to Xilinx document “DS181: Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics for the IO capabilities”.

Table 7-15 Pmod 1 FPGA Pin Assignments

Pmod 1 Pin	Signal Name	FPGA Bank_IO functions	FPGA Pin
1	PMOD1_0	B35_IO/0	R11
2	PMOD1_1	B35_IO/L2_P/T0/AD12_P	N9
3	PMOD1_2	B35_IO/L2_N/T0/AD12_N	M9
4	PMOD1_3	B35_IO/L3_P/T0/DQS_P/AD5_P	N8
5	GND		
6	VCC		
7	PMOD1_4	B35_IO/L3_N/T0/DQS_N/AD5_N	N7
8	PMOD1_5	B35_IO/L4_P/T0	M11
9	PMOD1_6	B35_IO/L4_N/T0	M10
10	PMOD1_7	B35_IO/L5_P/T0/AD13_P	P9
11	GND		
12	VCC		

Table 7-16 Pmod 2 FPGA Pin Assignments

Pmod 2 Pin	Signal Name	FPGA Bank_IO	FPGA Pin
1	PMOD2_0	B35_IO/L5_N/T0/AD13_N	P8
2	PMOD2_1	B35_IO/L6_P/T0	P6
3	PMOD2_2	B35_IO/L6_N/T0/VREF	N6
4	PMOD2_3	B35_IO/L7_P/T1/AD6_P	N1
5	GND		
6	VCC		
7	PMOD2_4	B35_IO/L7_N/T1/AD6_N	M1
8	PMOD2_5	B35_IO/L8_P/T1/AD14_P	M5
9	PMOD2_6	B35_IO/L8_N/T1/AD14_N	M4
10	PMOD2_7	B35_IO/L9_P/T1/DQS_P/AD7_P	R1
11	GND		
12	VCC		

NOTE: 5V IO devices are not supported. To avoid possible damage, do not connect peripherals with 5V IO levels to the Pmod IO receptacles.

7.13. General Purpose User LEDs

The TB-A7-200T-IMG has two rows of four user programmable LEDs, one row on each PCB side. Each LED in a row is parallel connected with a corresponding LED in the row on the other side of the PCB, hence there are 4 control signals used for all 8 LEDs. All eight LEDs are Green color, and the FPGA IOs drive active-high logic ("high" to turn on the LED and a logic "low" to turn it off). The user must ensure the FPGA configuration load contains definite IO states to the four LED signals as they must not be left floating after configuration is completed.

The following table details the FPGA IO assignment for driving the two LED groups. Note that they do not all originate from a single FPGA bank.

Table 7-17 User LEDs Pin Assignment

LED RefDes (top,bottom)	Signal Name	FPGA Bank_IO function	FPGA Pin
D11, D38	GRN_LED_1	B14_IO/L4_P/T0/D04	W28
D13, D39	GRN_LED_2	B14_IO/L4_N/T0/D05	W29
D14, D40	GRN_LED_3	B15_IO/25	U24
D15, D41	GRN_LED_4	B16_IO/25	M26

With PUDC_N (FPGA Bank 14 pin W26) pulled low, the LEDs all activate on power-up during FPGA configuration as the LED control signal IOs are pulled high internally. Note that this will not be the case if the optional PCB stuffing of PUDC_N (R84-in, R85-out) pulls the pin high to the Bank's VCCO. Under this condition, the LED control signals will float and any of the LEDs may or may not light up during configuration, depending on uncontrolled electrical characteristics.

7.14. General Purpose User Switches

7.14.1. User DIP Switches

The TB-A7-200T-IMG is equipped with two Copal Electronics CHS-04TA SPST 4-positions DIP switches. The switches are wired to pull the sensed IOs to logic “Low” in the ON position and read logic “high” when open.

Table 7-18 DIP Switches FPGA Pin Assignment

Switch RefDes	Signal Name	FPGA Bank_IO function	FPGA Pin
SW2	SWITCH1_1	B12_IO/0	AJ24
	SWITCH1_2	B12_IO/L22_P/T3	AM27
	SWITCH1_3	B12_IO/L22_N/T3	AN27
	SWITCH1_4	B12_IO/L23_P/T3	AL25
SW5	SWITCH2_1	B12_IO/L23_N/T3	AM25
	SWITCH2_2	B12_IO/L24_P/T3	AP25
	SWITCH2_3	B12_IO/L24_N/T3	AP26
	SWITCH2_4	B12_IO/25	AL24

7.14.2. User Push Switches

The board also features two sets of four C&K Components KMR211GLFS momentary push buttons. One set of 4 are on the PCB top, the other on the bottom directly underneath the top set. Each button is wired in parallel with its matching button on the other side, so all eight buttons are sensed with four IOs. In resting state, the sensed IOs read logic “high”; pressing a button, either top or bottom side, pulls the corresponding sense IO to logic “low”.

Table 7-19 Push-button Switches FPGA Pin Assignment

Push-button RefDes (top,bottom)	Signal Name	FPGA Bank_IO function	FPGA Pin
SW3, SW11	PUSHBUTTON_1	B14_IO/L6_N/T0/D08/VREF	Y28
SW4, SW12	PUSHBUTTON_2	B14_IO/25	W24
SW6, SW13	PUSHBUTTON_3	B13_IO/0	AD23
SW7, SW14	PUSHBUTTON_4	B13_IO/25	AF24

7.15. SPDIF Interface

The TB-A7-200T-IMG features a pair of SPDIF (Sony/Philips Digital Interface) COAX interconnect jacks, one for Transmit and the other for Receive. The jacks are industry standard RCA Phono style, designed to accept a 75-ohm COAX cable with an RCA style plug. The connector shells are industry standard Orange color that is commonly associated with wire (non-optical) consumer Digital Audio interface (i.e.: SPDIF). Transmit and Receive are identified by silkscreen text on the PCB top and bottom sides.

The 75-ohm line is supported using an Intersil ISL3176 RS-485 receiver/line driver device. Although the device supports differential line interface, both RX and TX are used in single-ended mode and are both AC coupled to the line. The line driver output level applied to the jack is adjusted to SPDIF specified level with an impedance matched resistive pad network. The schematic of the interface is shown below:

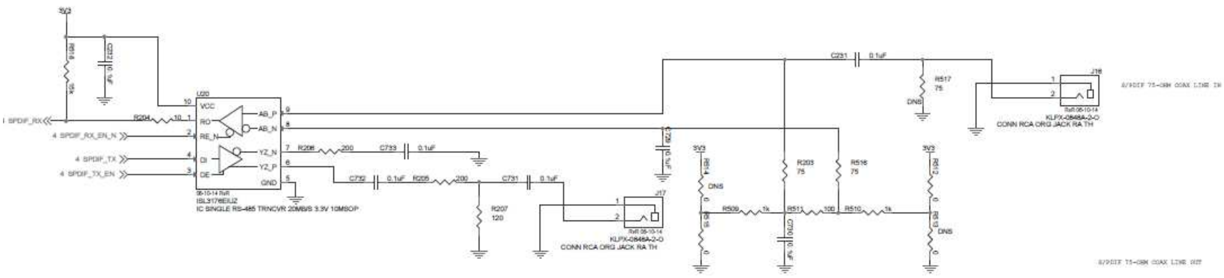


Figure 7-18 SPDIF Digital Audio Interface

The data on the line is presented in “true” logic where a rising transition on the FPGA output pin produces a rising transition on the line. The line is also received in “true” logic and no inversions are required prior to application to the FPGA input pin. In addition to the transmit and receive PHY function, the FPGA also controls both the receiver and transmitter enables to shut down the receiver/line driver device when not active. Note that the RX enable is active “low”, while the TX enable is active ”high”.

Table 7-20 SPDIF to FPGA Bank 35 Pin Assignment

Signal Name	SPDIF_RX	SPDIF_RX_EN_N*	SPDIF_TX*	SPDIF_TX_EN*
FPGA Bank 35 Pin	U10	T10	U7	U6

*Note: The SPDIF_TX and both EN signals must be defined in the FPGA code and not allowed to float. When the SPDIF_RX_EN_N is “high”, the SPDIF_RX signal is pulled “high”.

The SPDIF interface is tolerant of accidental reverse connection, however, the user must ensure that the source and destination are both SPDIF compliant to ensure correct operation. The input and output jacks present DC terminations: to avoid damaging the board, do not apply DC voltages greater than 2.5V on the receive port and 3V on the transmit port.

For more details on the electrical specification of SPDIF, refer to international standard IEC60958-3, Digital Audio Interface Part 3, Consumer Applications.

7.16. Fan Interface

The TB-A7-200T-IMG provides an active heatsink (fansink) for the FPGA since a full activation of all the GTP ports plus configurations full of high speed internal logic can readily push the device power consumption over 10W. The 3-pin fan connector J24 is located near the FPGA, and has a pinout that conforms to the Intel ATX standard.

The fan power comes from the main hot-plug protected 12V, and the fan's DC can be PWM modulated on the low side through an output of the FPGA. The Fan Tach signal represents the rotor speed and produces a pulse on each revolution. The Tach signal is provided to another IO on the FPGA, and can be used in a user designed fan control feedback loop that regulates the fan speed through PWM.

Table 7-21 Fan control to FPGA Pin Assignment

Signal Name	FPGA Bank_IO function	FPGA Pin
LS_FAN_TACH	B15_IO/0	T24
LS_FAN_PWM	B16_IO/0	L23

The PWM signal from the FPGA passes through the 90120A sequencer device which acts as a failsafe mechanism in case a design error or other cause would force the PWM signal to be held low (fan OFF). This is important since a dissipation of 10W in the FPGA can quickly raise the die temperature to damaging levels if the fan is not operating. An optional bypass strap (R582) is provided in case the user's PWM control logic includes failsafe provision and can be trusted enough to eliminate the 90120A protection. In that option, the user must ensure the PUDC_N (FPGA Bank 14 pin W26) is pulled low, so that the fan runs during FPGA configuration.

8. Default Settings

The TB-A7-200T-IMG contains a small number of user selectable settings, set by shorting shunts on headers.

Table 8-1 Default Jumper Configuration Selection by shunts across indicated pins

J12	J13	J14	J26	J40	J41	Selected Configuration
1-2	x	x	x	x	x	Enable Auto crossover, PHY SMBus address A4=1
x	N-A	1-2	x	x	x	Eth PHY TX CLK Delayed, RX CLK on RXD stable
x	x	x	x	3-4	x	FMC1 VADJ = 2.5V
x	x	x	x	x	3-4	FMC2 VADJ = 2.5V
x	x	x	none	x	x	FPGA configures from SPI Flash

9. Appendix A: EEPROM Contents

Currently not available.

TOKYO ELECTRON DEVICE

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